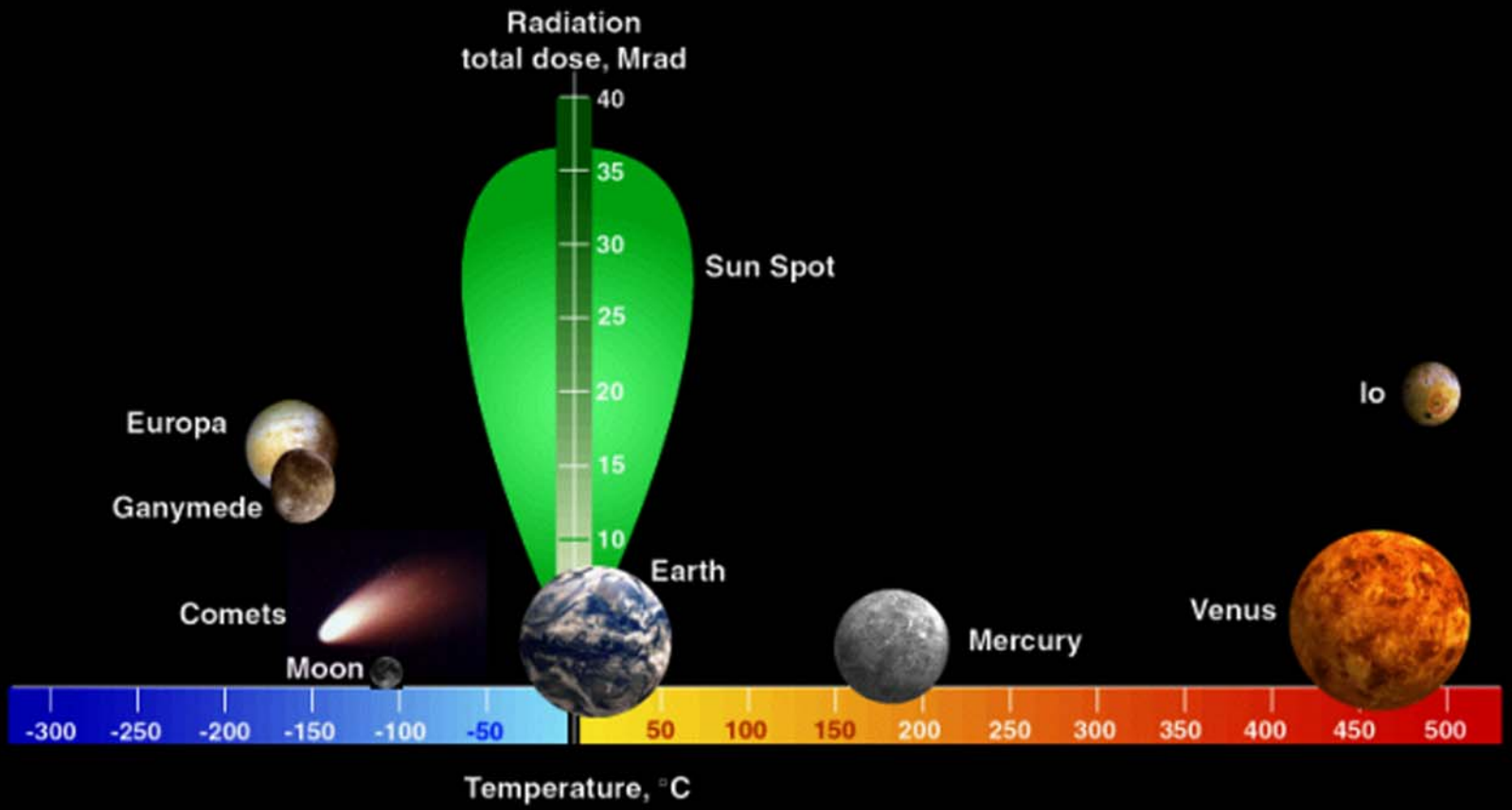
EEE LINKS

AUGUST 2002
VOLUME 8 NO. 2



NASA Electronic Parts and Packaging Program

Technology Information for Future NASA Missions

EEE Links, Volume 8, No. 2, August 2002
Focus on Extreme Environment Electronics

TABLE OF CONTENTS

Low and High Temperature Testing

- Evaluation of Data Retention and Imprint Characteristics of FRAMs Under Environmental Stresses for NASA Applications (Abstract)
  Ashok K. Sharma, NASA GSFC, and Alexander Teverovsky, QSS Group, Inc./NASA GSFC

- Reliability Evaluation of Thermally Actuated Micromachined Relays for Space Applications (Abstract)
  Alexander Teverovsky, QSS Group, Inc./NASA GSFC, and Ashok K. Sharma, NASA GSFC

- Effects of Extreme Temperature on Characteristics of Voltage Reference Microcircuits Encapsulated in Plastics (Abstract)
  Alexander Teverovsky, NASA GSFC/QSS Group, Inc.

- Evaluation of COTS Dual-Axis MEMS Accelerometers Before and After Extreme Temperature Thermal Cycling (-125 °C to 90 °C) (Report)
  Rajeshuni Ramesham, NASA JPL/Caltech, Ashok Sharma, NASA GSFC, and Alexander Teverovsky, QSS Group, Inc./NASA GSFC

- Assessment of Flip-Chip Advanced Test Assembly Electronics Packages Under Extreme Temperature Applications (Extended Abstract)
  Rajeshuni Ramesham, NASA JPL/California Institute of Technology

Very High Temperature SiC Based Packaging

- High Temperature Electronics: A Role for Wide Bandgap Semiconductors? (Abstract)
  Philip G. Neudeck, Robert S. Okojie, and Liang-Yu Chen, NASA GRC

- Microsystem Packaging for High Temperature Environments (Report)
  Liang-Yu Chen, OAI/NASA GRC, and Patrick McCluskey, University of Maryland, College Park

General Reports

- Characterizing Space-Flight Inductors and Transformer Failures (Abstract)
  Ben Oni, NASA MSFC/Tuskegee University, and Trent Griffin, Karen Cunningham, Bob Kapustka, and Steve Luna, NASA MSFC

DEPARTMENTS

Letter From the Editor

Jeanne A. Beatty
Editor of EEE Links
NASA GSFC, Greenbelt, MD 20771
jbeatty@pop500.gsfc.nasa.gov

Welcome to the August 2002 issue of EEE Links. I would like to thank the previous editor, Nancy Ford, for her contributions in making this newsletter the success it is today. EEE Links has become an important vehicle for NASA-wide information exchange regarding electronic packaging processes and parts news. Thanks also to the many authors who contributed to this issue. Please keep me informed about your questions and needs to enable me to best serve you. Suggestions and comments about the newsletter and its topics should be forwarded to my e-mail address cited above.

DEPARTMENTS

Guidelines for EEE Links Article Submission

EEE Links is a quarterly publication. The next publication date and focus will be:

December 2002 - Plastics
Article submission deadline is November 15, 2002.

Submitting articles for EEE Links is a great means by which to transfer information and knowledge inside and outside of the NASA community.

EEE Links supports the NASA Electronic Parts and Packaging Program (NEPP), and the information presented in this newsletter augments electronic parts, packaging, and radiation technologies.

EEE Links publishes many types of articles relevant to electronic parts, packaging, and radiation. Primary consideration is given to articles that relate specifically to the NEPP program, but we also consider articles outside of the NEPP program that address electronic parts, packaging, or radiation issues.

Article submissions can cover current efforts, referencing status and completion date. Articles can be informal and be from one paragraph to three pages in length on the following subjects:

- Current Events Within the NEPP Program and Projects
- Parts
- Packaging
- Radiation
- Reliability Issues Concerning NEPP
- New/Emerging Technology
- Space Flight Hardware
- Quality Assurance Issues.

To submit an article, please send it in a text-only format, preferably Microsoft Word, to Jeanne Beatty at jbeatty@pop500.gsfc.nasa.gov. Please provide the following information with your article submission:

- Abstract: This two- to four-sentence paragraph summarizes the key points to capture the reader's attention.
- Contact Information: The author must include his or her business address, phone, fax, and e-mail address.
- Notes and References: Most articles require some references, and some contain incidental information best treated as notes. Use brackets for references and superscripts for notes, then list the two groups separately at the end of the article. These should be numbered in the order in which they appear in the article, not alphabetically.

- Additional Reading: Our readers appreciate pointers to relevant books and articles. List these at the end of the article in the same format as the references.
- Copyright: The author is responsible for obtaining any copyright releases or other releases necessary for their article. The releases should be forwarded to the EEE Links Editor (see Jeanne Beatty's e-mail address above).
- Biography (to be supplied when requested): This should be between 50 and 75 words outlining the author's job, background, professional accomplishments, and other pertinent accolades or areas of interest. Accompanying photographs might be requested also; these should either be in .gif or .jpg format if possible.

Letters to the Editor

Please limit letters to 250 words. Include your name, phone number, and e-mail address. Names are withheld from publication upon request. We reserve the right to edit for style, length, and content.

DEPARTMENTS

Upcoming Events

International Wafer-level Packaging Conference
August 22, 2002, Four Points Sheraton, 1250 Lakeside Drive, Sunnyvale, CA
For details, contact Bette Cooper, info@meptec.org, 650.988.7125, or see Web site http://www.mepteconline.com/

Standing Independent Review Board (SIRB) (Invitation Only)
August 27 to 28, 2002, NASA Headquarters, Code Q, Washington, DC
For details, contact Tom Whitmeyer, Code Q, 202.358.2228

Airspace/Airline Plating Forum Expo (The American Electroplating and Surface Finishers Society)
August 27 to 29, 2002, Raddison Hotel, Orlando, FL
For details, contact Douglas B. Wyatt, http://www.aesf.org, 407.281.6446, or see Web site http://www.aesf.org/conferences/aerospace.html

IMAPS 2002—35th International Symposium (Microelectronics)
September 4 to 6, 2002, Colorado Convention Center, Denver, CO
For details, contact Jackie Morris-Joyner, jmorris@imaps.org, 305.382.8433, or see Web site http://www.imaps.org

IMAPS 2002 (Fundamentals of Hybrid Microelectronics Professional Development Course)
September 6, 2002, Adam's Mark Hotel, Denver, CO
For details, contact Rayma Gollopp, rgollopp@imaps.org, 202,548.8711, or see Web site http://www.imaps2002.org

IMAPS 4th Advanced Technology Workshop (Packaging of MEMS and Related Micro Integrated Nano Systems
September 6 to 8, 2002, Adam's Mark Hotel, Denver, CO
For details, contact Jackie Morris-Joyner, jmorris@imaps.org, 305.382.8433

International KGD Packaging and Test Workshop
September 8 to 11, 2002, Napa, CA
For details, contact Larry Gilg, exhibits@napakgd.com, 512.452.0077, or see Web site http://www.napakgd.com

2002 MAPLD International Conference (The 5th Annual MAPLD)
September 10 to 12, 2002, Kossiakoff Conference Center, Johns Hopkins University, Baltimore, MD
For details, contact Richard Katz, mapld2002@klabs.org, 301.286.9705, or see Web site mapld2002@klabs.org

National Fiber Optic Engineers Conference
September 15 to 19, 2002, Dallas Convention Center, Dallas, TX
For details, contact NFOEC, info@nfoec.com, 1.973.829.4832, or see Web site http://www.nfoec.com

Semicon Taiwan
September 16 to 18, 2002, Taipei World Trade Center, Taipei, Taiwan
For details, contact Customer Service, customerservice@semi.org, 1.408.943.7919, or see Web site http://www.Semi.org

IPC International Conference on Unique Interconnections
September 18 to 19, 2002, Montreal, Canada
For details, contact IPC, http://www.ipc.org, 847.509.9700

Optoelectronics Packaging and Micro-opto-electromechanical Systems (MOEMS)
October 8 to 11, 2002, Bethlehem, PA
For details, contact Rajeshuni Ramesham, rajeshuni.ramesham@jpl.nasa.gov, 818.354.7190, or see Web site http://www.imaps.org

International Test Conference (ITC) 2002
October 8 to 11, 2002, Baltimore Convention Center, Baltimore, MD
For details, contact Jill Sibert, j.sibert@advantest.com, 610.758.8190

IMAPS Advanced Technology Workshop
October 11 to 14, 2002, Radisson Hotel, Bethlehem, PA
For details, contact Bill Heffner, wheffner@agere.com, 202.548.4001, or see Web site http://www.imaps.org/callfor/atw2001opto.htm

The 28th International Symposium for Testing and Failure Analysis
November 3 to 7, 2002, Phoenix Civic Plaza, Phoenix, AZ
For details, contact David Dylis, ddylis@iitri.org, 315.337.9932, or see Web site http://www.edfas.org/istfa

DEPARTMENTS

Up Close With Hasso Niemann

EEE Links interviewed Dr. Hasso Niemann, Head of the Atmospheric Experiment Branch (Code 915) at NASA Goddard Space Flight Center, to provide system and mission level views of extreme environment electronics and to speculate on future missions with regard to extreme environment issues. This perspective complements the extreme environment parts and packaging applications and reliability issues focus set forth in this issue from our EEE Links authors. Dr. Niemann received his Ph.D. in Electrical Engineering from the University of Michigan in 1969 and has been with Goddard since then. He is renowned worldwide as the authority on developing atmospheric composition measurement techniques using space flight mass spectrometry. The Galileo Probe Mass Spectrometer is the latest in a number of outstanding achievements by Dr. Niemann in his distinguished career; he ensured that the design and construction of the probe's mass spectrometer could accommodate Jupiter's strenuous environment, and he won the 1997 John C. Lindsay Memorial Award for his role as Principal Investigator in this work.

EEE Links: What do you foresee for the future of NASA missions to such planets as Venus, Mars, and beyond?

Dr. Niemann: Devices designed to operate in extreme environments are in high demand within NASA's planetary activities. NASA is currently conducting extreme environment workshops at JPL on in-situ instruments involving spectrometry to measure chemical compositions of atmosphere and soil. Because of the in-situ character, most instruments in planetary research must be able to withstand very hot and cold environments.

The National Research Council has recently released the Solar System Exploration Decadal Survey, "New Frontiers in the Solar System: An Integrated Exploration Strategy." It reviews the current state of planetary science and exploration and makes recommendations for ground-based and space flight research for the years 2003 to 2013. Key recommendations include maintenance of the Discovery program (low cost, one every 18 months, plus extending the Cassini mission), beginning a New Frontiers line of missions (medium cost, one every 3 years, such as KBO/Pluto Explorer, Lunar South Polar Aitken Basin Sample Return, Jupiter Polar Orbiter with Probes, Venus In-Situ Explorer, and Comet Surface Sample Return), and one large-cost mission (Europa Geophysical Explorer), as well as recommendations for the Mars Explorer Program. The full report can be accessed at http://www.nationalacademies.org/ssb/.

EEE Links: What are the most significant challenges regarding extreme environment in these missions?

Dr. Niemann: Major environmental challenges are temperature, pressure, chemical reactions in the atmospheres (e.g., Venus), and of course radiation. Areas of interest include Venus' surface and atmosphere; this planet is similar to Earth in some ways, but its atmosphere is dense—there is as much as 100 times more pressure on Venus than on Earth—and it has a hostile high temperature atmosphere of 500 °C with traces of corrosive sulfuric acid. We need to revisit this atmosphere and take more measurements; the challenge posed here is that we need our instruments to survive operation at 500 °C. The electronic devices we have used could survive the environment only for a short time before they were destroyed. To make more detailed measurements, we need extended survival time for the instruments, and that requires greater temperature tolerance. This problem is being worked on; NASA Glenn Research Center is well known for their research in high temperature electronics.

EEE Links: To accomplish these missions, what new materials, technologies, and approaches would be necessary?

Dr. Niemann: High temperature and low temperature electronics, as well as other areas like micro-electromechanical systems, are key technologies that need to be advanced. Certain MEMS technology is especially important because those devices are small and well suited for high temperature environments. Nanotechnology may also play an important role in the future; currently it is being developed primarily in biological areas using biotransistors and so on that are not easy to use in extreme environments, but they could be packaged to avoid temperature effects. We don't know enough now about the reliability of nanotechnology so it is not on the immediate agenda.

In future Mars missions, we will use drilling techniques to get surface soil samples, as the interesting matter (water, or even life) is most likely to be under the surface. Another approach is sample return, in which an instrument or spacecraft collects samples and brings them back to Earth for very detailed analysis.

In the semiconductor area, high temperature materials such as gallium nitride and silicon carbide are needed that can withstand high temperature environments. In the mechanical area, titanium and possibly carbon fiber materials technology needs to be developed, and efficient cooling techniques that can cool or shield critical components by surrounding them. If the instrument's lifetime is expected to be short, shielding it to prevent it from reaching the high temperature and pressure of the environment becomes most important. Miniaturization is key in this, as small instrument devices can be shielded more effectively.

The other extreme is cold temperature applications for outer planets, which include Saturn, Jupiter, and their moons; for these we need small, low temperature electronic devices. The atmosphere of Saturn's moon Titan is not much different from ours on Earth, which makes it important for study, except for that it has 1.5 times Earth's surface pressure and is 90 °K to 100 °K. We don't know yet what the surface is made of, but it is probably covered with hydrocarbon

and frozen methane/ethane, so we would need low temperature electronics to explore that surface.

EEE Links: What sort of sensor/detector requirements and operational temperature ranges are relevant to these missions?

Dr. Niemann: The most significant requirement is for sensors to be effective where the environment is different from the state in which the measurements can be made; for example, on Venus, the instrument that makes the measurements is operating at a pressure many orders of magnitude below that of the ambient surface pressure. To reduce the sampling pressure for a mass spectrometer, by for example 10 orders of magnitude, is technically problematic. Also, in the optical area, there are problems with coating on lenses, contamination, and sulfuric acid corrosion. Materials that resist corrosion like high chromium-type alloys, titanium, and even certain types of stainless steel are being used.

EEE Links: How feasible is landing on Venus and making measurements? How long would the instrument last?

Dr. Niemann: Landing on Venus is very feasible and has been done by the Russians and NASA. Limited survival time of perhaps several hours is technically achievable using current technology. Pioneer Venus Probes that landed more than 20 years ago, survived for nearly an hour. Sample returns will follow the in-situ studies; they will involve, for example, landing a probe on the surface, collecting the samples, inflating a balloon to lift the package to a higher altitude, and firing off a rocket that is then captured by an orbiter and brought back to Earth. JPL is currently studying variations on this type of scheme.

EEE Links: What is the science objective for studying Mars?

Dr. Niemann: The Mars mission objective is under intensive study now, especially after finding traces of ancient life. Origin, climate, evolution are all major science objectives. In our group, atmospheric chemistry and dynamics and surface composition are under study (heavy ice has been discovered on the polar cap), and to confirm findings directly, probes must be placed there. We are looking for water and hope to find evidence of past or present biological activity by drilling several meters down below the surface.

EEE Links: How does extreme environment tie into NASA's two major enterprises, Space Sciences and Earth Sciences?

Dr. Niemann: The instrumentation and scientific experiments are similar in Space and Earth studies, but the advantage for Earth Sciences is that we can afford to fly much larger instruments because they are not going very far from Earth. Also, communication is much easier, so we can get higher data rates.

EEE Links: How can the NEPP Program, with its emphasis on device parts and packaging, address some of the extreme environment challenges?

Dr. Niemann: MEMS, SOI, SiC, and gallium nitride are all technologies that tie into NEPP goals. The packaging itself needs to be examined; ASICS is now popular, but we need analog ASICS. Passive components like electrolytic capacitors are still very vulnerable to temperatures. We would like to do MEMS mass spectrometry and have electronics on the same chip; the small size presents quite a challenge. Communication systems are in the same category—they also need to be miniaturized. Miniaturization is of course less important for instruments that do require large apertures, although smaller and lighter electronics packages would still be very desirable.

Introduction: NASA Extreme Environment Parts and Packaging Applications and Reliability Issues

Ashok K. Sharma, NASA GSFC, Code 562
Ashok.K.Sharma.1@gsfc.nasa.gov

This issue of the NASA Electronic Parts and Packaging Program (NEPP) EEE Links is focused on extreme environment electronics; it contains summaries, abstracts, and test reports from the NEPP Group. Research from NASA GSFC, JPL, GRC, LaRC, and MSFC is represented, as well as from universities and contractor partners.

NASA has ongoing programs and missions planned for the future that require operation of planetary probes, payloads, and instruments over a wide temperature range, such as below -125 °C for the Martian environment to over 500 °C for the Venusian atmosphere. Microsystems composed of microelectronics and micro-electro-mechanical systems (MEMS) are being considered increasingly for high temperature applications such as aerospace engine monitoring and space exploration. NASA projects such as Next Generation Space Telescope (NGST), Mars Exploration Rover (MER), and Mars Smart Lander (MSL) require operation at very low temperatures—all the way down to cryogenic temperatures (e.g., 4.2 °K for sensor elements). A probe launched for Asteroid Nereus will be exposed to temperatures ranging from -180 °C to 100 °C. Reliable cold electronic systems capable of operating at cryogenic temperatures will be needed for many future NASA space missions, including deep space probes and spacecraft for planetary surface explorations.

The military specifications for microelectronic components used in probes and planetary exploration mission flight hardware encompass a maximum operating temperature range of -55 °C to +125 °C. Commercial-off-the-shelf (COTS) devices, which are also being used increasingly in these missions, have a specified operating temperature range of only -30 °C to +85 °C. Hazards posed by extreme environments entail high doses of cumulative radiation (total ionizing dose), as well as single event phenomenon (SEP) that includes single event upset (SEU), single event latchup (SEL), and single event gate rupture (SEGR). In addition, various elements of the environment, such as low temperature and total dose exposure, can combine to create even greater problems. Therefore, it is of great interest to the NASA community to evaluate performance and reliability characteristics of military/commercial temperature range devices over extreme environments and provide guidelines for applications, packaging, and risk mitigation techniques.

Many of these extreme environment application challenges and reliability issues are being addressed by the NEPP program. The NEPP Cold Temperature Electronics Group including JPL, GRC, and GSFC has performed evaluation on several technologies and part types of interest. For example, GRC is currently investigating the effects of cryogenic temperature and thermal cycling effects on DC-DC converters that are widely used in space power systems for power management, conditioning, and control. In addition to the DC-DC converter testing, GRC has also tested COTS plastic encapsulated voltage references and power switching devices. GSFC has performed low/high temperature testing on MEMS accelerometers, thermally actuated micromachined relays, evaluation of data retention and imprint characteristics of FRAMs under environmental stresses, and characterization of extreme temperature effects on plastic encapsulated voltage reference microcircuits. JPL has performed extreme low temperature characterization of rad-hard and commercial quad receivers and A-D converters.
For additional details, see the full report posted on the NEPP Web site at
http://nepp.nasa.gov/index_nasa.cfm/619/09FE38FB-17FA-4D11-8CD3C71ABE5B8D16/.

NEPP Parts and Packaging Cold Temperature Electronics Task Team Report and Their Findings

Reza Ghaffarian, NASA JPL
Reza.Ghaffarian@jpl.nasa.gov

A NASA-wide team that has been working on characterization of cold electronics parts and packages reported their findings in an internal JPL report (JPL D-20434). The team collaborated under the NASA Electronic Parts and Packaging Program (NEPP) to characterize electrical and package robustness of newly available (technologies that are available commercially) and advanced (technologies that may soon be available commercially) electronic parts/packages and assemblies under extreme cold environment that represent current and future needs of NASA. Extreme environments are extended nominal operating temperature regimes specified by the manufacturers. Understanding the effects of extended thermal cycling is a long-term process, but it is crucial to evaluate new systems with advanced technologies for future space missions in the context of stringent safety and reliability. Extended thermal cycling in the range of hundreds of cycles is being performed currently, and test results will be presented in a subsequent document. The electronic packages assembled with various parts must be validated over a wide temperature range in order to infuse such technology into future space missions.

Electronic and radio subsystems on the Mars Exploration Rovers (MER), Nanorovers to Asteroid (MUSES CN), Next Generation Space Telescope (NGST), or other NASA missions must be maintained presently at a near constant temperature with heating elements installed as a part of the microelectronic package/system. Heating the electronic system boards requires and consumes a considerable amount of power. Operating such subsystems under ambient conditions experienced on Mars or an asteroid, such temperature controls could be eliminated, providing added flexibility in the overall design of future rovers. Most previous research in the area of low temperature electronics has been highly limited to work on cold temperature of -55 °C for military applications, and a limited amount of work has been done below this temperature, such as the boiling point of liquid nitrogen (-196.6 ^{o}C or 76.6 ^{o}K) or liquid helium (-269 ^{o}C or 4.2 ^{o}K) temperatures. Rover electronics and electronic packages would be exposed to ambient temperatures on Mars ranging from -125 ^{o}C to +40 ^{o}C and on the asteroid Nereus ranging from -180 ^{o}C to 100 ^{o}C. Perhaps the most vital issue in addressing the effects of cold temperatures on spacecraft electronic packages is the thermal variation associated with exposure to the ambient conditions on the surface of Mars and an asteroid.

Commercial-off-the-shelf (COTS) electronic packages such as Honeywell gate arrays, SRAMs, EEPROM, CMOS operational amplifiers, P channel MOSFETS, N channel MOSFETS, pull up resistors, surface mount resistors, NPO ceramic 0.1 mF capacitors, Harris 8-bit flash converters, high dielectric ceramic capacitors, and printed wiring board (PWB) materials were planned to be used on the Nanorover board for the MUSES CN project. The Nanorover MUSES-CN stands for Mu Space Engineering Spacecraft – C (indicates third in series), and N (indicates NASA). This project was a part of the Japanese mission to an asteroid 4660 Nereus, which involved plans to use electronic parts/packages beyond the envelope given by the suppliers/manufacturers. The MUSES CN group worked with the NEPP Cold Electronics Team to obtain the assessment of both their parts/package and board level assembly needs. The team narrowed their findings to a key task that can be completed within a limited budget, identified several parts/packages, and

designed and assembled a board with an SRAM. Temperature cycling ranges were extended by the requirement of MUSES CN to provide meaningful information for other NASA missions.

Wherever possible, the NEPP Cold Electronics Team, which consists of Electronic Parts Project, Electronic Packaging Project, and Electronics Radiation Characterization Projects within JPL and at other NASA Centers provided a comprehensive solution to NASA hardware projects. The primary objective of the NEPP projects is to evaluate newly available and advanced electronic parts/package technologies in order to enable effective support of NASA-wide requirements. Individual tasks funded under NEPP used their respective resources to accomplish overall objectives of the project; this helps shape NEPP activities to not only align with the needs of NASA's programs and projects, but also to facilitate interdependent work within NASA. The Centers currently involved in this project include Glenn Research Center (GRC), Langley Research Center (LaRC), and Jet Propulsion Laboratory (JPL).

The JPL internal report includes but is not limited to characterization, validation, assessment, and development of test methods/tools for specific parts/packages and assemblies at extreme environments in supporting missions of NGST, MER, and Mars Smart Lander (MSL), etc.

Parts/package and assemblies characterized and reported include the following:

- RS422 Rad-hard Quad Receivers, HS26C32RH, Linear Technology's LTC 1419A (plastic), Space Electronics Inc.'s SEI 7872 A/D, Intersil's HS 9008 RH A/D, and Stanford Microdevices' SLN 543 IF.

- Assemblies of three-challenger kit board/package used as part of Quality Assurance JPL Training Center. Assemblies entail several package types, including ball grid array (BGA). A board was designed and built to test Honeywell's HX6228 SRAM.

Several electrical parameters were characterized at discrete temperatures to -185 °C to determine whether they remain within their specification ranges. Both packages and boards were subjected to nondestructive testing including optical, X-ray, and acoustic microcopy to document their integrity prior to environment exposure. Package/board assemblies were also subjected to X-ray to characterize solder joint integrity, including void levels. Both parts and assemblies were subjected to thermal cycling with a large temperature swing enveloping numerous NASA missions. Details on testing and results are presented.

Cryogenic Evaluation of an Advanced DC/DC Converter Module For Deep Space Applications

Richard Patterson, NASA GRC, Richard.L.Patterson@grc.nasa.gov
Malik E. Elbuluk, University of Akron, Akron, Ohio 44325
Scott Gerber, ZIN Technologies, 3000 Aerospace Parkway, Brook Park, Ohio 44142
Ahmad Hammoud, QSS Group, Inc., NASA GRC, Cleveland, Ohio 44135

Background

Electronic circuitry and power systems designed for deep space applications and outer planetary exploration are required to operate reliably and efficiently under extreme temperature conditions. This requirement is dictated by the fact that the operational environments associated with some of the space missions would encompass temperatures as low as -183 °C. The development and utilization of electronics capable of low temperature operation would not only fulfill the advanced technology requirements, but also would contribute to improving circuit performance, increasing system efficiency, and reducing development and launch costs. These benefits are generally achieved by the improved intrinsic properties of some of the electronic materials at low temperature, reduced device losses, and the elimination of heating elements used in conventional systems at low temperatures.

The Low Temperature Electronics Group at NASA Glenn Research Center (GRC) is currently performing investigation on the effects of cryogenic temperature and thermal cycling on electronic devices and circuits. These activities are pursued in collaboration with other NASA Centers and Jet Propulsion Laboratories (JPL) in support of the NASA Electronic Parts and Packaging (NEPP) Program. DC/DC converters are widely used in space power systems in the areas of power management, conditioning, and control. In this work, the performance of an advanced commercial DC/DC converter was investigated under low temperature. The converter module was investigated in terms of its output voltage regulation, efficiency, and ripple characteristics. These properties, which were determined in the temperature range of -140 °C to 20 °C, were obtained at various load levels and at different input voltages. Some of the experimental data obtained are presented in this summary. More detailed information is presented in a NASA internal white paper [1], and the full report will be posted on the NEPP Web site.

Experimental Investigation

The investigated commercial-off-the-shelf modular DC/DC converter has a power rating of 10 W with an input voltage range of 16 V to 40 V and an output voltage of 3.3 V, and is space qualified in terms of radiation tolerance. Its operating temperature range is specified between -65 °C to 70 °C. The converter module was investigated in terms of its output voltage regulation, efficiency, and ripple characteristics. These properties were determined in the temperature range of -140 °C to 20 °C. At a given temperature, these properties were obtained at various input voltages and at different load levels from no-load to full-load conditions. The tests were performed as a function of temperature using an environmental chamber cooled by liquid nitrogen. A temperature rate of change of 10 °C/min. was used throughout this work. The modular converter was tested at the following temperatures: 20, 0, -20, -40, -60, -80, -100, -120,

and -140 °C. At every test temperature, the test article was allowed to soak for a period of 30 minutes before any measurements were made. After the last measurement was taken at the lowest temperature, the converter was allowed to stabilize to room temperature, and then the measurements were repeated at room temperature.

The output voltage and efficiency of the converter at various load levels is shown in Figure 1 as a function of temperature. These parameters are obtained utilizing an input voltage of 24 V. The converter exhibited good voltage regulation with temperature down to -100 °C. This trend was maintained regardless of the load level to which the converter was subjected. Below -100 °C, however, the converter started to display inconsistent behavior in its voltage regulation. At any given test temperature, the efficiency increased as the load was increased. At temperatures below -100 °C, the efficiency was at minimum as the converter exhibited some loss in output regulation.

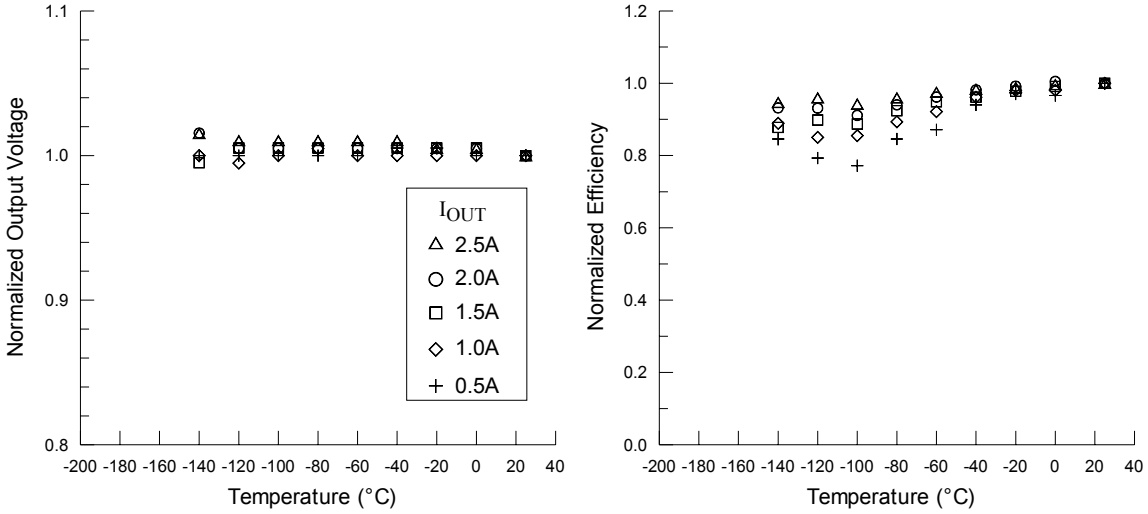


Figure 1. Output voltage and efficiency versus temperature at various loads (input voltage = 24 V).

The converter displayed the same behavior in its voltage regulation and efficiency with an applied input voltage of 40 volts, as shown in Figure 2. Once again, the efficiency, at a given test temperature, had the highest value when the maximum loading level was applied to the converter. At temperatures below -140 °C, regardless of the input voltage level, the converter exhibited complete loss in output regulation. This trend, however, reversed when the test temperature was brought above -140 °C.

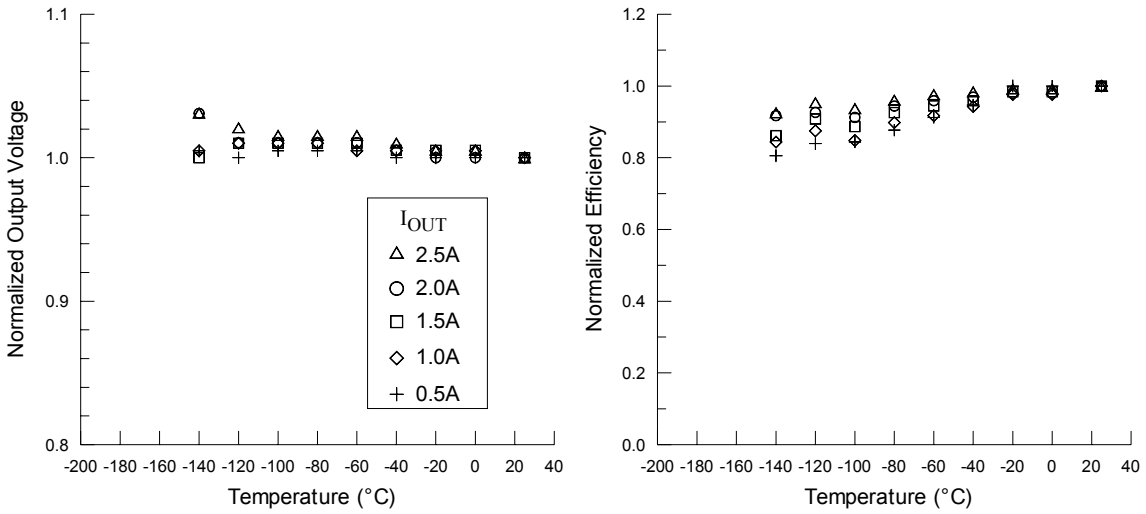


Figure 2. Output voltage and efficiency versus temperature at various loads (input voltage = 40 V).

Waveforms of the converter output voltage and current ripple, and the input current ripple at room temperature (25 °C) and at a low temperature (-100 C) are shown in Figures 3 and 4 for light load and heavy load, respectively. Theses waveforms were obtained using an input voltage of 16 V. No effect of temperature can be observed as no significant variations occurred in either the frequency or the amplitude of the investigated properties.

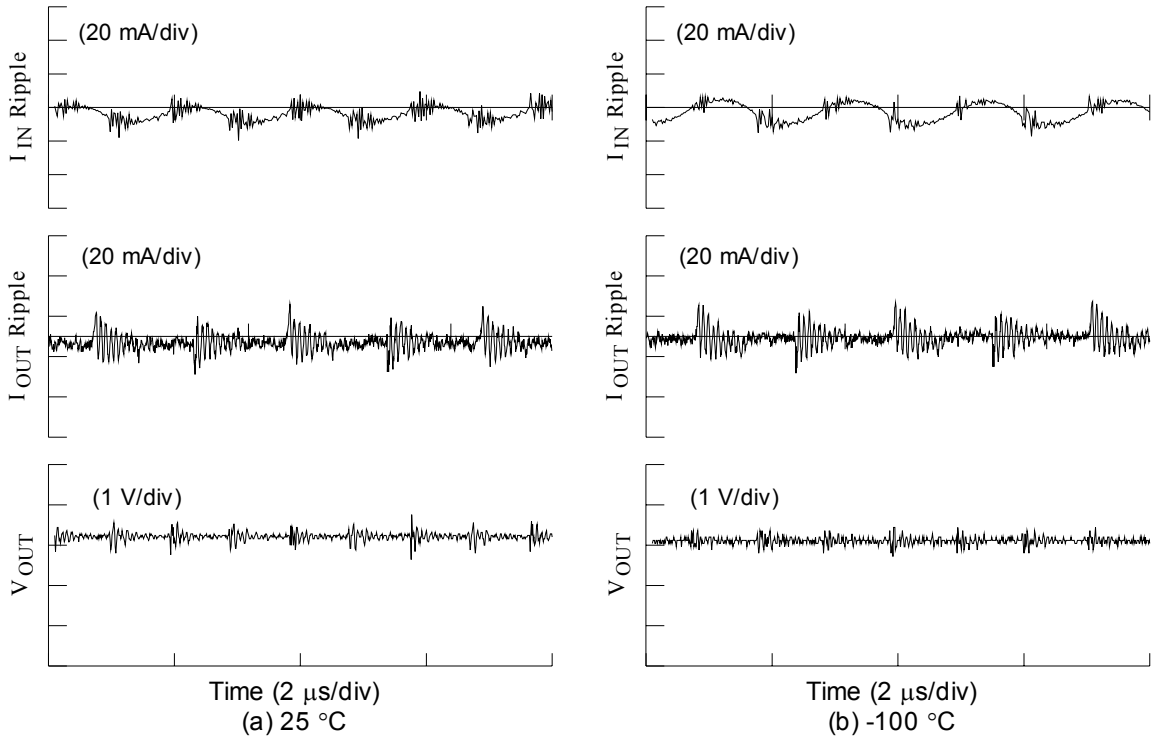


Figure 3. The converter ripple characteristics at low input voltage (16 V) and under light load (1.0 A) at two temperatures.

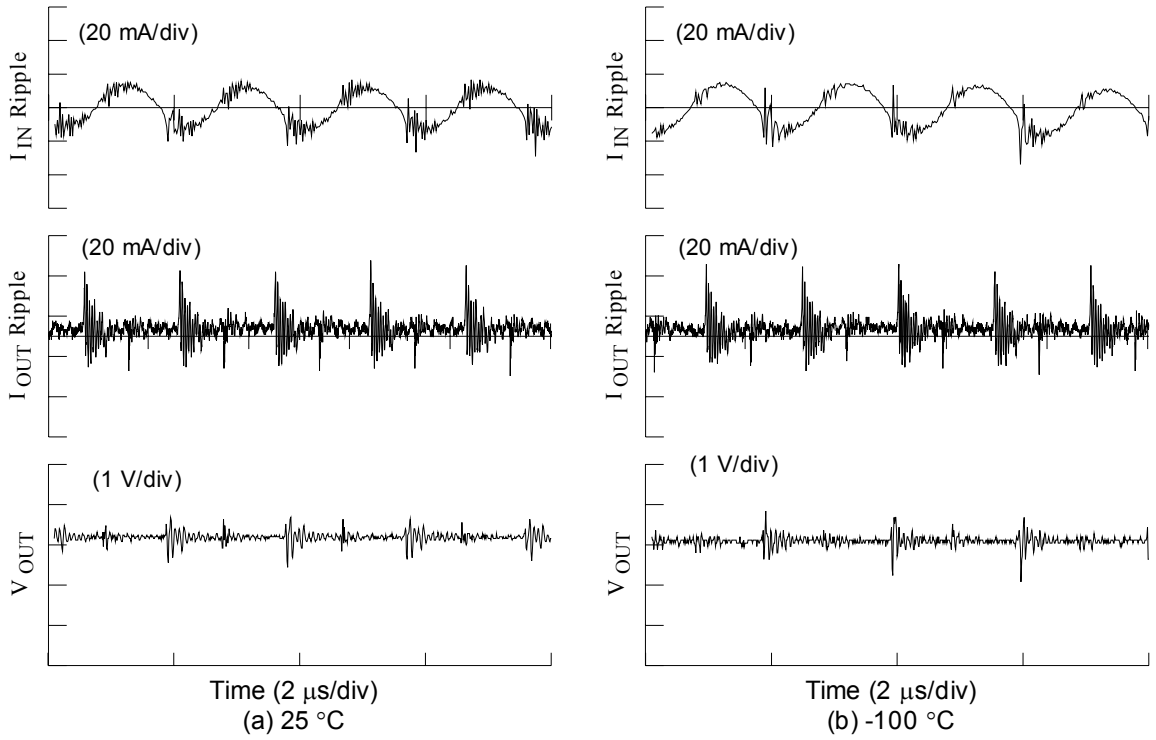


Figure 4. The converter ripple characteristics at low input voltage (16 V) and under heavy load (2.5 A) at two temperatures.

Conclusion

An advanced radiation-hardened DC/DC converter was characterized in terms of its performance as a function of temperature in the range of -140 °C to 20 °C. The converter was evaluated with respect to its steady state output voltage regulation, efficiency, output voltage ripple, input current ripple, and output current ripple at various input voltage levels and loads. In general, this converter displayed good performance in regulation, efficiency, and dynamic characteristics with temperature down to -100 C. Some instability was observed as the temperature was decreased further. More testing under long-term thermal exposure is needed to fully characterize this converter for potential application in low temperature environments.

Acknowledgement

This work was performed under NASA Glenn Research Center GESS Contract #NAS3-00145. Support for this work was provided by the NASA Electronic Parts and Packaging (NEPP) Program. The authors acknowledge the support given by Dr. Michael Newell of JPL's NEPP Electronic Parts Project.

References

[1]. "Cryogenic Evaluation of an Advanced DC/DC Converter Module for Deep Space Applications," internal NASA white paper.

Evaluation of Voltage Reference Circuits and N-Channel Field Effect Transistors at Low Temperatures

Richard Patterson, NASA GRC, Richard.L.Patterson@grc.nasa.gov
Ahmad Hammoud, QSS Group, Inc./NASA GRC
Scott Gerber, ZIN Technologies, 300 Aerospace Parkway, Brook Park, Ohio 44142

Background

Many deep space and planetary exploration missions require power electronic components and systems that can operate reliably and efficiently in cryogenic temperature environments. Some of these missions include Mars Exploration Rovers (MER), Next Generation Space Telescope (NGST), Europa Orbiter, and Galaxy Explorer (GALEX), to name a few. Presently, spacecraft and probes operating in the cold environment of deep space carry on-board an accessory heating system in order to maintain an operating temperature for the electronics of approximately 20 °C. Electronics capable of operation at cryogenic temperatures will not only tolerate the hostile environment of deep space, but also reduce spacecraft size and weight by eliminating the heating units and associated structures, thereby reducing system development and launch costs, improving reliability, and increasing lifetime.

In a collaborative effort between NASA's Glenn Research Center (GRC), Goddard Space Flight Center (GSFC), and the Jet Propulsion Laboratory (JPL) under the NASA Electronic Parts and Packaging (NEPP) Program, the effects of extreme temperature and thermal cycling on various electronic devices and circuits are being investigated. This summary presents some of the results obtained on the evaluation of voltage reference and power switching devices under extreme temperature exposure.

Voltage Reference Circuits

Two circuit boards, populated with different voltage reference integrated circuit (IC) chips and a few passive components, were designed and built for evaluation in the temperature range of +25 °C to -180 °C. The circuits were characterized at test temperatures of 25, 0, -40, -80, -100, -120, -140, -160 and -180 °C in a liquid nitrogen cooled environmental chamber. Limited thermal cycle testing was also performed [1-2]. The plastic-packaged voltage reference IC chips were comprised of Linear Technology LT1461 and Analog Devices AD780BR. The LT1461 device is a low dropout micropower bandgap voltage reference with low drift and very high accuracy. The device draws very little current (35 μA) and is capable of providing an output drive current of 50 mA [3]. The low supply current makes it ideal for low power and portable applications, and its output current capability makes it suitable for high power requirements such as power supplies, analog-to-digital and digital-to-analog converters, and precision regulators. The device provides a steady output of 2.5 V from inputs up to 20 V, and it is specified for operation from -40 °C to +125 °C. The AD780BR counterpart is an ultrahigh precision bandgap voltage reference that can provide a pin-programmable output of 2.5 V or 3.0 V from inputs between 4.0 V and 36 V. It can be used to improve the performance of high-resolution analog-to-digital and digital-to-analog converters due to its capacitive-load driving capability. The device is specified for operation from -40 °C to +85 °C with low temperature drift and low output noise [4]. A

temperature output pin provided on the AD780 allows the device to be configured as a temperature transducer while providing a stable output reference voltage. It is capable of sourcing or sinking up to 10 mA and can be used in series or shunt mode, thus allowing positive or negative output voltages without external components. The two devices were evaluated in terms of their 2.5 V output voltage regulation under a wide range of input voltage. These characteristics were obtained at various temperatures and at three different load levels.

Figure 1 shows the deviation in the output voltage of the LT1461 device with respect to its room temperature value. The data, which is shown as a function of temperature, is depicted for input voltages of 3, 12, and 20 volts at three different load levels. It can be seen that the reference output voltage generally remains within specifications (2.499 to 2.501 V) between temperatures of 25 °C to -40 °C. Below -40 °C, however, the output voltage begins to fluctuate as the temperature is decreased. While the output voltage undergoes a slight increase with decrease in temperature for the no-load condition, it exhibits a decrease when a load is applied. The intensity of this drop in the output voltage seems to depend on both the levels of the input voltage and the applied load. For example, the decrease is most dramatic at the highest load level with input voltages of 12 and 20 volts, as seen in Figure 1. In addition, the beginning of this trend occurs at temperatures as low as -80 °C, as compared to -120 °C for the case of other load/input voltage combinations. Furthermore, the device exhibits unstable operation at the two extreme low temperatures of -160 °C and -180 °C. Instability was also observed at temperature as low as -80 °C only when an input voltage of 3 V was applied under high load condition. It is important to note that at test temperature of -180 °C, the device completely loses its voltage regulation and it tends to behave almost like a unity-gain amplifier stage.

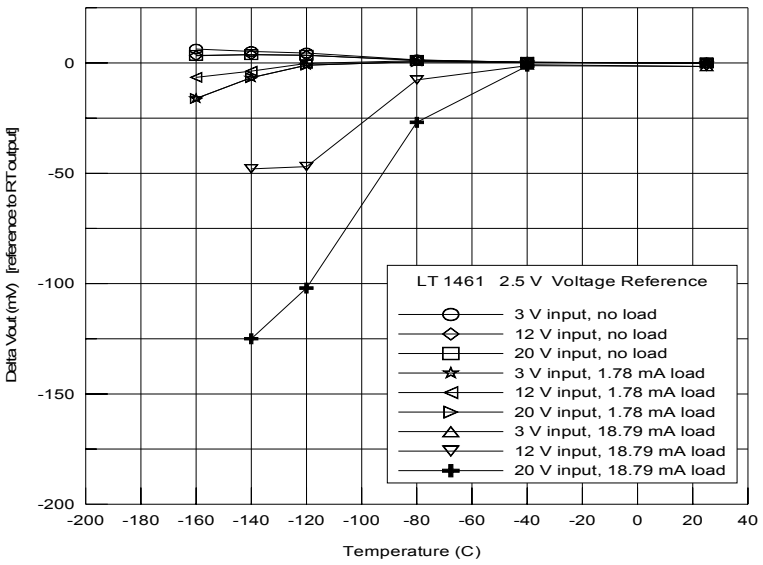


Figure 1. Deviation in output of LT1461 versus temperature at different test conditions.

The deviation in the output voltage of the AD780BR device with respect to its room temperature value is shown in Figure 2. The data, which is shown as a function of temperature, is depicted for all input voltage and load level combinations. It can be seen that the reference output voltage remains within specifications (2.499 to 2.501 V) between temperatures of 25 °C to -40 °C.

Between -40 °C and -120 °C, however, the output voltage begins to decrease very slowly as the temperature is decreased. In addition, the device exhibits unstable operation at the two extreme low temperatures of -160 °C and -180 °C. Instability was also observed at the test temperature of -140 °C only when an input voltage of 4 V was applied under no load condition. It is important to note that if the output specifications were broadened to cover a range of 2.495 V to 2.501 V, the device would be useful down to temperatures of -120 °C.

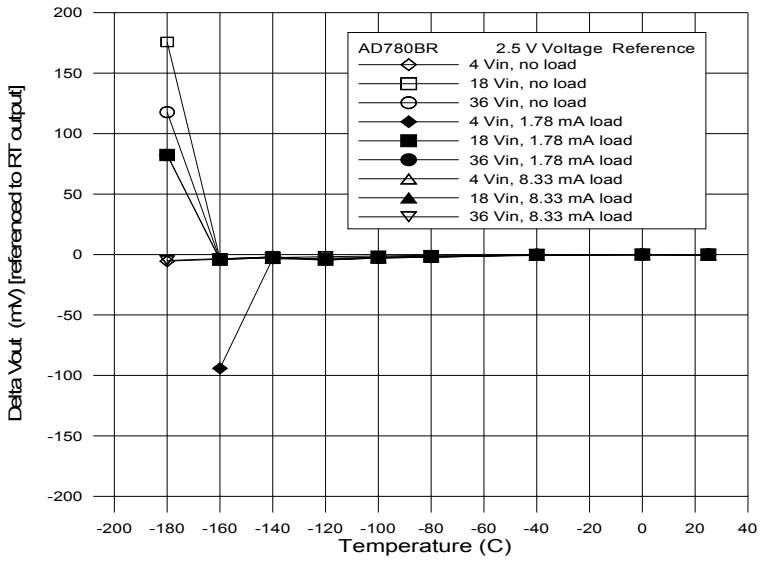


Figure 2. Deviation in output of AD780 versus temperature at different test conditions.

Power Switching Devices

An N-channel Silicon-On-Insulator (SOI) power field effect transistor (FET) device, Honeywell HTANFET, along with a control device (a standard "non-SOI" power FET), International Rectifier IRFD110 HEXFET Power MOSFET, were characterized in the temperature range of +20 °C to –190 °C. Performance characterization was obtained in terms of their gate threshold voltage (VGS[th]), drain-to-source on-state resistance (RDS[on]), and drain current (ID) versus drain-to-source voltage (VDS) family curves at various gate voltages (VGS). These properties were obtained using a digital curve tracer. The test temperatures at which these devices were investigated were: 20 °C, -50 °C, -75 °C, -100 °C, -125 °C, -150 °C, -175 °C, and -190 °C. Limited thermal cycling testing was also performed on the devices. These tests consisted of subjecting the devices to a total of five thermal cycles between +20 °C and -190 °C. Table I shows some of the operating specifications for the HTANFET and IRFD110 devices tested.

Figure 3 shows the output characteristics of the IRFD110 MOSFET at room temperature (20 °C). The output characteristics are defined as drain current (ID) versus drain-to-source voltage (VDS) family curves at various gate voltages (VGS). Gate voltages (VGS) utilized were 3.0V to 8.0V in steps of 0.5V. Note that no output was obtained with VGS equal to 3.0V, which is below the gate threshold voltage of 3.03 volts. Figure 4 shows the output characteristics of the same device at -190 °C. Two temperature-induced effects can be noted in the output characteristics of the device with change in the test temperature. The first is the downward shift

of the VGS curves due to the increase in the gate threshold voltage with decreasing temperature. There is also a leftward shift of the VGS curves, especially at VGS ≥ 6.0V. This shift is primarily due to the decrease in on-state resistance with decreasing temperature.

Table I. Manufacturer's specifications of devices tested [5-6].

Device	Symbol	Parameter	Rating	Units
HTANFET	$T_{(oper)}$	Operating temperature	–55 to +225	°C
	I_D	Continuous drain current	* 1 max	A
	$V_{(BR)DSS}$	Drain-source breakdown voltage	* 90 min	V
	$R_{DS(on)}$	Drain-to-source on-state resistance, V_{GS}=5V & I_D=0.1A	* 0.4 typ	Ω
	$V_{GS\ (th)}$	Gate threshold voltage	* 1.6 typ * 2.4 max	V
	$V_{GS\ (max)}$	Maximum gate-to-source voltage	10	V
IRFD110	$T_{(oper)}$	Operating temperature	–55 to +175	°C
	I_D	Continuous drain current	* 1 max	A
	$V_{(BR)DSS}$	Drain-source breakdown voltage	* 100 min	V
	$R_{DS(on)}$	Drain-to-source on-state resistance, V_{GS}=10V & I_D=0.6A	* 0.54 max	Ω
	$V_{GS\ (th)}$	Gate threshold voltage	* 2.0 min * 4.0 max	V
	$V_{GS\ (max)}$	Maximum gate-to-source voltage	20	V

* Operating condition T = 25 °C.

The output characteristics of the HTANFET SOI MOSFET at room temperature are shown in Figure 5. Gate voltages (VGS) utilized in this test were between 1.5V to 6.0V. Once again, a VGS level exceeding the gate threshold voltage value must be applied for the device to produce any output. Figure 6 shows the output characteristics of the same device at -190 °C. Similar to its IRFD110 counterpart, the HTANFET device exhibited changes in its output characteristics with temperature. These changes, which are reflected by the shift and steepness of the family curves, are attributed to the increase in the gate threshold voltage and the decrease in the on-state resistance as temperature is decreased.

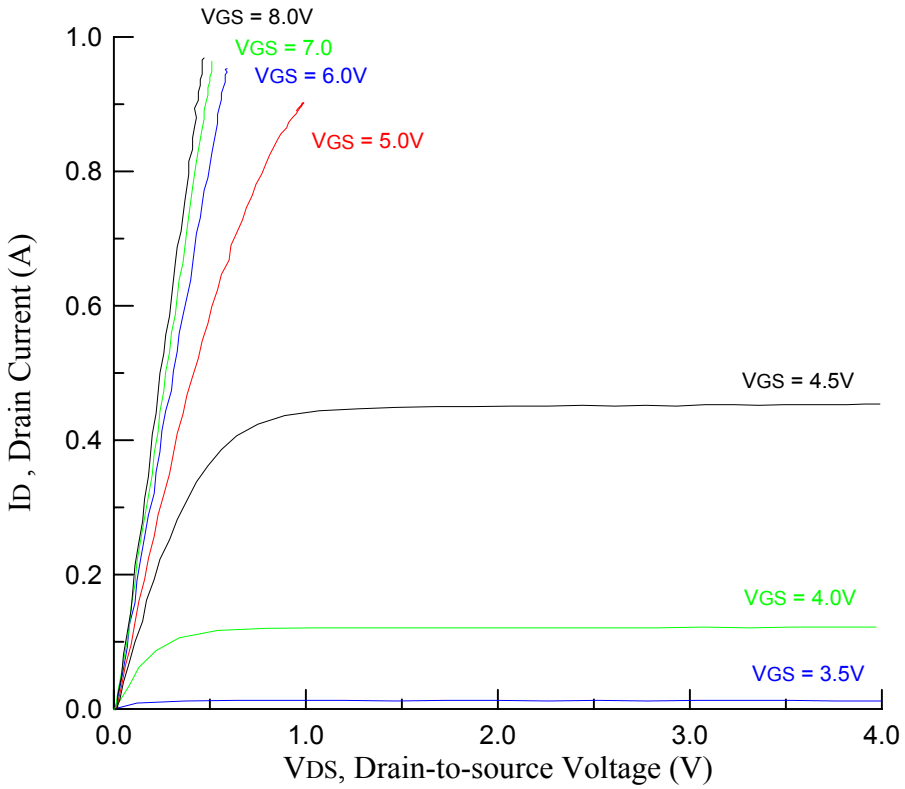


Figure 3. Output characteristics of the IRFD110 device at 20 °C.

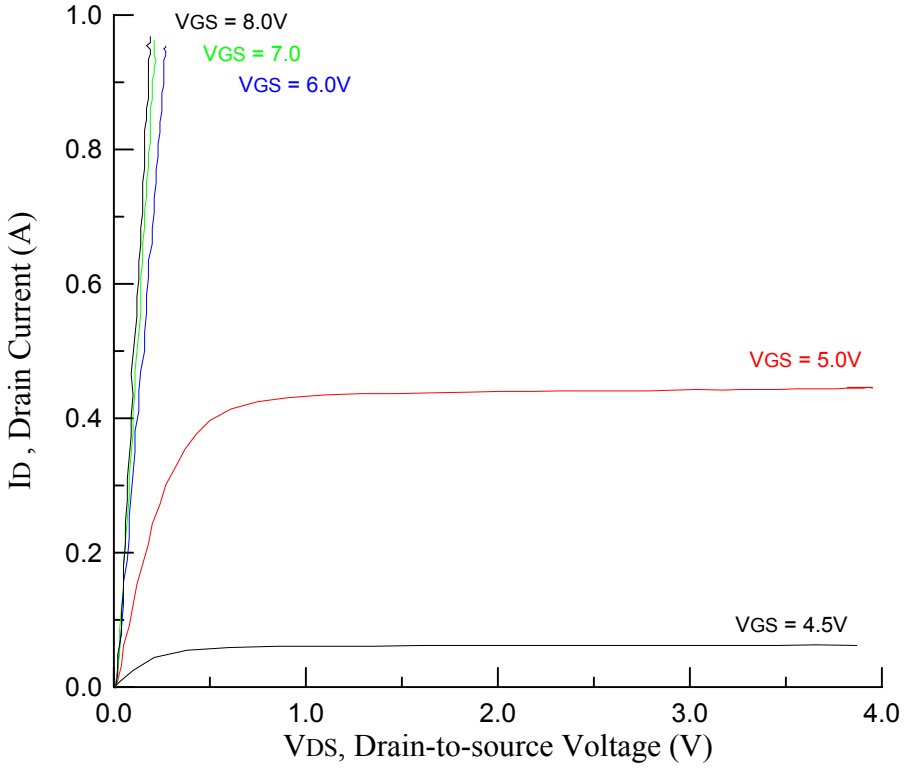


Figure 4. Output characteristics of the IRFD110 device at -190 °C.

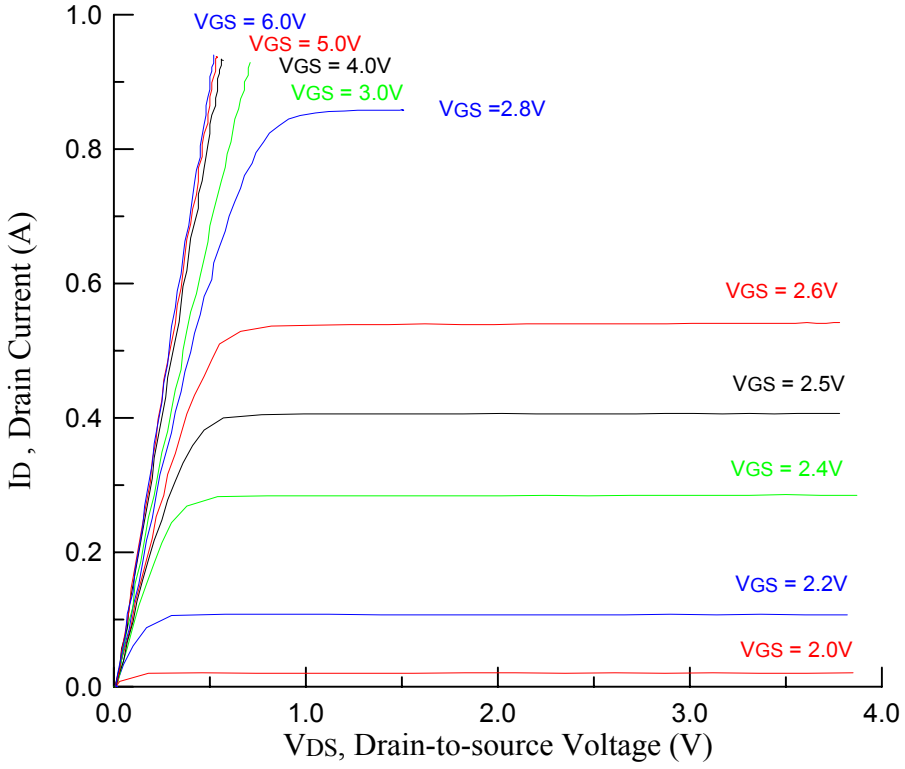


Figure 5. Output characteristics of the HTANFET device at 20 °C.

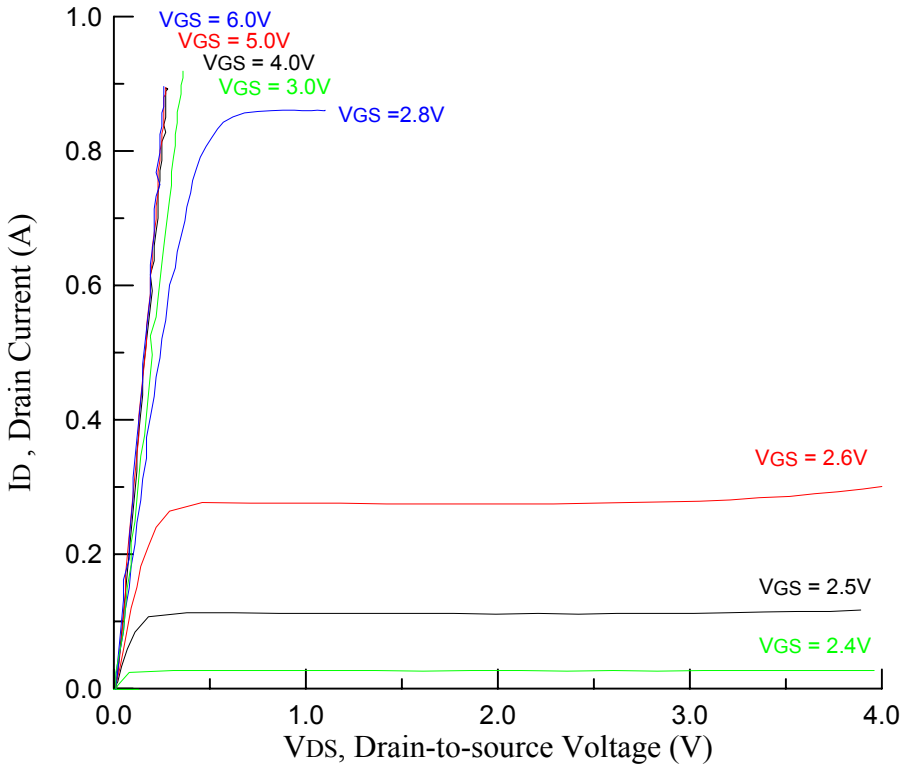


Figure 6. Output characteristics of the HTANFET device at -190 °C.

Limited thermal cycling (five cycles between +20 °C and -190 °C) of both devices appeared not to influence their characteristics as no changes occurred in the operational behavior of either device. For example, the pre- and post-cycling values of both the gate threshold voltage and the on-state resistance of the two devices remain almost the same as shown in Table II.

Table II. Effects of thermal cycling on gate threshold voltage (VGS[th]) and on-state resistance (RDS[on]).

	$V_{GS(th)}$ (V)		$R_{DS(on)}$ (Ω)	
Device	Before (20 °C)	After 5 cycles (20 °C)	Before (20 °C)	After 5 cycles (20 °C)
IRFD110	3.03	3.04	0.49	0.48
HTANFET	1.64	1.65	0.58	0.59

Remarks

An ongoing Low Temperature Electronics Program at the NASA Glenn Research Center focuses on the development of electronic devices and systems geared for operation under extreme temperatures in deep space applications. Major activities in this program include characterization and reliability assessment of advanced and commercial-off-the-shelf (COTS) components and circuits for use in low temperature environments. Extensive collaboration and coordination exist with the NASA Electronic Parts and Packaging (NEPP) and the NASA Electronic Parts Assurance Group (NEPAG) Programs in pursuing these efforts.

References

1. "Evaluation of Linear Technology LT1461 Voltage Reference at Low Temperature," NASA GRC white paper.
2. "Performance of Analog Devices AD780BR Voltage Reference at Cryogenic Temperatures," NASA GRC white paper.
3. Linear Technology LT1461-2.5 Micropower Precision Low Dropout Series Voltage Reference Data Sheet.
4. Analog Devices AD780 High Precision Reference Data Sheet, Rev. B.
5. HTANFET High Temperature N-Channel Power FET Data Sheet, Honeywell.
6. IRFD110 HEXFET Power MOSFET Data Sheet, International Rectifier.

Acknowledgments

This work was performed under the NASA Glenn Research Center GESS Contract # NAS3-00145. Support was provided from the NASA Electronic Parts and Packaging (NEPP) Program, EPAC Task "Effects of Wide Temperature Exposure on Characteristics of Plastic Encapsulated COTS Components for Space Applications" and EPAC Task "Reliability of Cold Interconnects." The authors acknowledge the support of Dr. Reza Ghaffarian and Dr. Rajeshuni Ramesham of NASA JPL, and Dr. Ashok Sharma of NASA GSFC.

Note: This document summarizes the following three full-length test reports, which are posted on the NEPP Web site: Low Temperature Evaluation of the HTANFET Silicon-on-Insulator (SOI) N-Channel Field Effect Transistor, Performance of the Analog Devices AD780BR Voltage Reference at Cryogenic Temperatures, and Evaluation of the Linear Technology LT1461 Voltage Reference at Low Temperatures. Respectively, they can be accessed at http://nepp.nasa.gov/index_nasa.cfm/619/3B717CDF-DFF7-473D-850D1467C0C91C21/, http://nepp.nasa.gov/index_nasa.cfm/619/36AA56DF-052E-496B-AD0FB4E51537354E/, http://nepp.nasa.gov/index_nasa.cfm/619/32152DC5-86BC-4222-84E6BA27FD442279/.

Evaluation of Data Retention and Imprint Characteristics of FRAMs Under Environmental Stresses for NASA Applications

Ashok K. Sharma, NASA GSFC
Ashok.k.Sharma.1@gsfc.nasa.gov

Alexander Teverovsky, QSS Group Inc./NASA Goddard Operations
Alexander.Teverovsky@gsfc.nasa.gov

Terry W. Dowdy, NAVSEA Crane
dowdy_t@crane.navy.mil

Abstract

A major reliability issue for all advanced nonvolatile memory (NVM) technology devices including FRAMs is the data retention characteristics over an extended period of time, under environmental stresses and exposure to total ionizing dose (TID) radiation effects. These advanced memories are mostly available as commercial-off-the-shelf (COTS) devices and often use the latest submicron technologies, new dielectric materials, multi-layer interconnect processes, and advanced plastic packaging. In the NVMTS 2001, data retention and fatigue characteristics of 64 Kb PZT-based FRAMs from Ramtron Corp., tested over a temperature range from -85 °C to +310 °C for ceramic packaged parts and from -85° C to +175 °C for plastic parts, during retention periods of up to several thousand hours, were reported. The observed data retention failures were divided into three categories: (1) random failures that were not related to stress conditions, (2) weak cell failures, which were also not related to a particular stress condition but were reproducible from test to test, and (3) intrinsic failures that were caused by thermal degradation (or wearout) of the ferroelectric cell material. A conclusion was that additional testing should be performed on higher density 256 Kb FRAMs.

For this additional testing, 256 Kb FRAMs in 28-pin plastic DIPs, rated for an industrial grade temperature range of -40 °C to +85 °C, were procured. These are two-transistor, two-capacitor (2T-2C) design FRAMs. In addition to data retention characteristics, the parts were also evaluated for imprint failures, which are defined as the failure of cells to change states (e.g., from 1 to 0, or 0 to 1) and are somewhat similar to hysteresis effect.

These 256 K FRAMs were subjected to scanning acoustic microscopy (C-SAM); 1,000 temperature cycles from -65 °C to +150 °C; high temperature aging at 150 °C, 175 °C, and 200 °C for 1,000 hours; highly accelerated stress test (HAST) for 500 hours; 1,000 hours of operational life test at 125 °C; and total ionizing dose radiation testing. As a preconditioning, 10 K read/write cycles were performed on all devices. Interim electrical measurements were performed throughout this characterization, including special imprint testing.

Failures were observed during high temperature aging testing at 200 °C, during HAST testing, and during 1,000 hours of operational life at 125 °C. The parts passed 20 Krad exposure, but there were failures during post-30 Krad electrical measurements. Test results and failures analysis will be presented at the Non-Volatile Memory Technology Symposium, NVMT'02 and posted on the NEPP Web site when they have been completed.

Reliability Evaluation of Thermally Actuated Micromachined Relays for Space Applications

Alexander Teverovsky, QSS Group, Inc./NASA Goddard Operations, 301.286.6216
Alexander.A.Teverovsky.1@gsfc.nasa.gov

Ashok K. Sharma, NASA GSFC, 301.286.6165
Ashok.k.Sharma.1@gsfc.nasa.gov

Micromachined relays combine benefits of solid-state devices, such as low size, weight, power consumption, and time response with conventional electromechanical relays, such as low leakage currents and high radiation hardness. MEMS switching devices do not generate spurious signals at high frequencies and have low insertion losses, high linearity, and broad bandwidth, which is advantageous for developing RF and microwave frequency systems. These features make micromachined relays very attractive for space applications, especially for a new generation of small and nano-satellites.

One of the major reliability concerns in MEMS switches is contact sticking. In this respect, thermally actuated relays have advantages over electrostatic relays. The actuation mechanism in thermally activated devices creates significant mechanical forces during opening and closing, which overwhelms potential adherence forces and micro-welding of metal contacts.

This paper reports results on quality and reliability evaluation of the first micromachined relays commercially available from Cronos. The parts have been characterized in a wide range of temperatures (from -100 °C to +160 °C) and load conditions (voltages from 10 V to 100 V and currents from 0 mA to 200 mA).

Mechanical integrity of the parts has been evaluated by subjecting them to multiple mechanical shocks in the range from 100 G to 1,000 G (Fig.1). Life testing was performed at different load conditions during more than 10^8 switching cycles. Figures 2 to 4 illustrate some results of the life testing.

To evaluate conditions that cause contact failures, experiments with capacitance discharge through the contacts were performed. The values of capacitance changed from 4.7 μF to 47 μF, the load resistance varied from 3 Ohm to 100 Ohm, and the voltage across the capacitors was incrementally increased from 1 V to 200 V. The results (Fig. 5) could be explained based on a simple energy dissipation model and allowed for estimation of critical energy required to cause contact failures.

It is known that low-pressure conditions can cause failures in conventional electromechanical relays [1]. For the thermally actuated MEMS relays, vacuum was found also to be a detrimental environment. All observed failures were caused by overheating of the polysilicon heaters (see Figures 6 and 7) and were due to a reduction of heat dissipation in the actuator under vacuum conditions.

Typical failure mechanisms associated with different test conditions (see Figures 7 through 9), as well as the processing and manufacturing defects, are discussed. The detailed test results will be reported and posted on the NEPP Web site when they have been completed.

[1]. A. Teverovsky, Relay Failures Specific to Space Applications, ISTFA'99, Proceedings from the 25th International Symposium for Testing and Failure Analysis, 1999, Santa Clara, CA, pp. 285-292

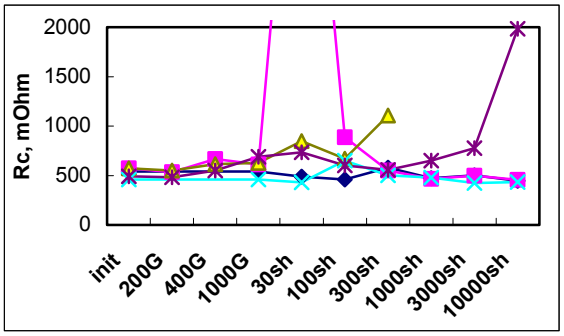


Fig. 1. Mechanical shock test results. No failures after 10 shocks 400G.

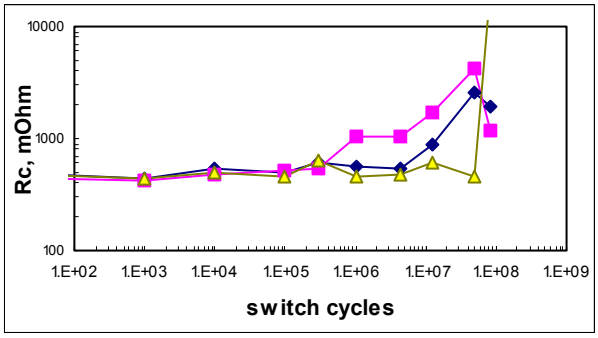


Fig. 2. Contact resistance variation during life test cycling. No load conditions.

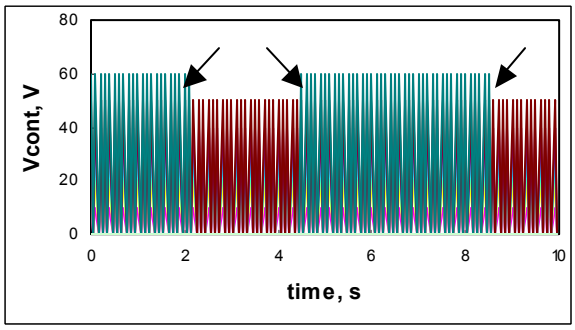


Fig. 3. Intermittent failures at 60V/2mA during 100 pulses step test.

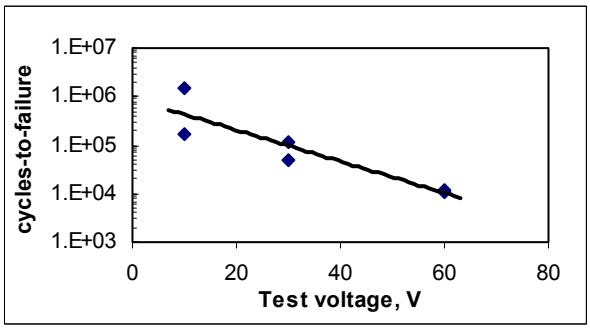


Fig. 4. Resistive load life test at different contact voltages.

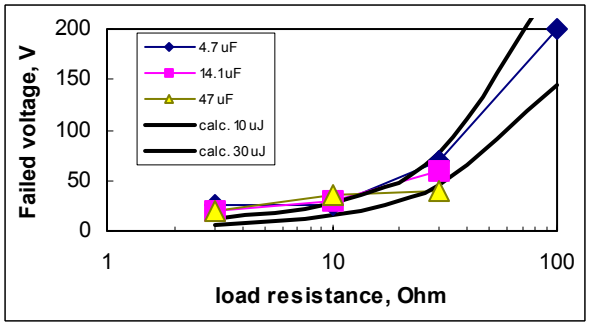


Fig. 5. Capacitance discharge step test. Marks indicate experimental data, solid lines – calculations.

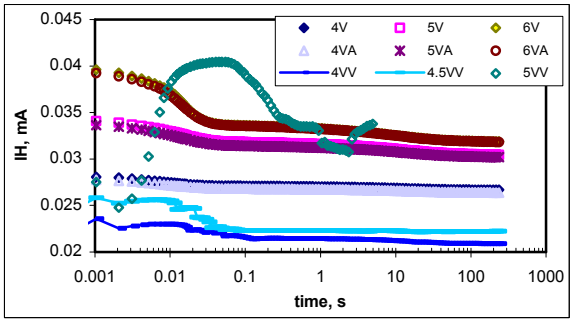


Fig. 6. Kinetics of heating currents at normal conditions and during failure in vacuum.

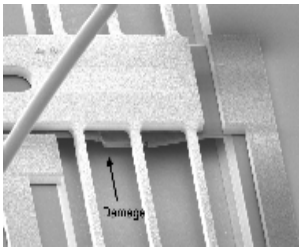


Fig. 7. Failure of the heater during vacuum testing.

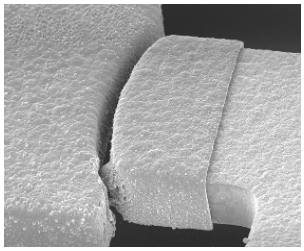


Fig. 9. Failed contacts after life test cycling at 60V, 10 mA.

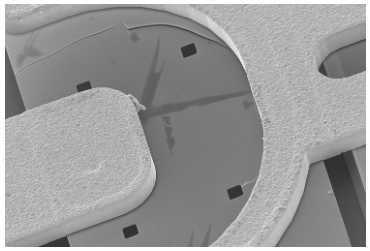


Fig. 8. Cracks in polysilicon after mechanical shock testing.

Effects of Extreme Temperatures on Characteristics of Voltage Reference Microcircuits Encapsulated in Plastics

Alexander Teverovsky, QSS Group, Inc./NASA Goddard Operations
Alexander.A.Teverovsky.1@gsfc.nasa.gov
301.286.6216
NASA GSFC, Code 562, Greenbelt, MD 20771

Abstract

Temperature excursions can change mechanical stresses in plastic encapsulated microcircuits (PEMs) and cause parametric shifts (temperature hysteresis) in characteristics of linear devices. Exposure of linear PEMs to extreme temperatures during deep space missions might cause significant errors and failures in sensitive circuits. However, this phenomenon, its temperature dependence, and the rate of relaxation have not been adequately investigated, in particular, as applicable to voltage reference microcircuits.

In this work, characteristics of precision voltage reference PEMs (Linear Technology LT1461 and Analog Devices AD780 AR and BR parts) have been evaluated in the temperature range from -120 ^{o}C to +160 ^{o}C. Parametric shifts as a result of extreme temperature excursions were measured at room temperature and monitored during long-term relaxation at temperatures from room to +85 ^{o}C.

Results showed that without load, the output voltage of the parts remain within +3,000 ppm tolerance at temperatures up to +160 ^{o}C and -3,000 ppm at temperatures down to -120 ^{o}C. However, under the load (Iout = 10 mA) failures occurred at temperatures below -100 ^{o}C and above +140 ^{o}C. It has been shown that even a short-term (15 minutes) low temperature (-65 ^{o}C to -120 ^{o}C) exposure of the parts causes output voltage shift of 100 to 200 ppm, which is large enough to cause failures in sensitive systems with resolutions of 12 bits and higher. Excessive moisture content in the molding compound of the package increases parametric shifts after the low temperature exposure to 500 – 700 ppm. Measurements within 1,000 hours did not reveal any significant relaxation in the voltage output at temperatures below ~75 ^{o}C. A physical mechanism of the parametric shift is discussed.

This work was performed as a part of NEPP PEMs' evaluation activities, and the full report will be posted on the NEPP Web site when it has been completed.

Evaluation of COTS Dual-Axis MEMS Accelerometers Before and After Extreme Temperature Thermal Cycling (-125 ^{o}C to 90 ^{o}C)

Rajeshuni Ramesham, NASA JPL/Caltech, Rajeshuni.Ramesham@jpl.nasa.gov
Ashok Sharma, NASA GSFC, Ashok.K.Sharma.1@gsfc.nasa.gov
Alexander Teverovsky, [3] QSS Group, Inc./NASA GSFC, Alexander.Teverovsky@gsfc.nasa.gov

Abstract

Analog Devices ADXL 250 and 202, dual-axis, surface micromachined accelerometers were subjected to extreme environmental thermal cycling, beyond the manufacturer's specifications of -65 ^{o}C to 150 ^{o}C, to evaluate the robustness of devices and packaging. The extreme environmental thermal cycling conditions were established as follows: (a) Total number of cumulative thermal cycles = 61; (b) temperature range of -125 ^{o}C to 90 ^{o}C; (c) ramp rate of 7 ^{o}C/minutes; and (d) dwell time of 10 minutes on each of the cold and hot sides. A non-destructive X-ray evaluation technique was used to image the accelerometers before and after thermal cycling. Functional tests were performed during temperature cycling, and failures were observed in some of the accelerometers. Analysis of the failed devices is still in progress, and results will be reported later.

Introduction

Micro-electromechanical systems are some of the most recent advanced technologies in microelectronics, which have paramount importance to military and aerospace applications. Accelerometers are the earliest and the most developed representatives of MEMS, which have been under use for air bag deployment applications in automobiles for more than a decade. The accelerometer sensitivity required for aerospace or military applications varies from 80,000 G to 10^{-6} G, and the applications include ballistic munitions launches, deep space probes, and attitude and position control. The presence of moving parts in MEMS, which are fabricated by using a surface micro-machining process on the surface of a silicon substrate, dictates a reliability assessment towards cycling fatigue of micro-mechanical components under extreme temperatures or beyond manufacturer specifications. Fatigue damage of micro-mechanical components will certainly influence the performance of the MEMS devices. Environmentally induced failures generated via thermal cycling are of significant importance to NASA if one can understand and mitigate the failures by improving the design.

Temperature Profile

Figure 1 shows the temperature profile employed to perform the extreme temperature thermal cycling of the ADXL 250 and the boards with ADXL 202 accelerometers.

ADXL 250 and 202

Analog devices ADXL 250 and 202 are dual axis surface micro-machined accelerometers rated for ±50 G and packaged in a hermetic 14 lead surface mount cerpack. The operating temperature range of these accelerometers is -55 ^{o}C to 125 ^{o}C and storage temperature range is from -65 ^{o}C to

150 ^{o}C. Figure 2 shows optical photographs of the some of the test vehicles with ADXL 202 and ADXL250 accelerometers.

Electrical Tests

ADXL accelerometers have a limited number of parameters specified, including sensitivity for X and Y channels, self test for X and Y channels measured as output change, and quiescent supply current. Tables 1 and 2 show the electrical characteristics of the several accelerometers after 27 and 61 cumulative thermal cycles, respectively. The sensor number 38 has failed after 27 thermal cycles as per data in Table 1. Failure analysis of this is still in progress. No further failures were observed after 61 cumulative thermal cycles as noted the results in Table 2.

X-ray Imaging

Fein focus X-ray imaging technique has been used to image the sensors and boards before and after thermal cycling. Figures 3, 4, and 5 show the X-ray images of the ADXL 202 and 250 before and after thermal cycling. No noticeable changes were observed in the X-ray images. X-ray imaging of sensor #38 will be performed to determine whether any failures internal to the package can be detected. No external cracking was observed as a function of thermal cycling. No damage was observed at the interconnects as a function of thermal cycling as per images in Figures 3 through 5.

Conclusions

Analog Devices ADXL 250 and 202 accelerometers were subjected to extreme temperature thermal cycling such as -125 ^{o}C to 90 ^{o}C. X-ray images of the sensors were taken before and after thermal cycling for 61 cycles. There were no physical failures observed externally or internal to the package. Only one sensor failed after 27 thermal cycles. At present we do not have destructive failure analysis (DPA) on the failed sensor device. This work is still continuing, and any noticeable findings will be reported in the future.

Acknowledgements

Thanks are due to Mr. Steve Bolin for his help in X-ray imaging prior to and after thermal cycling of the accelerometers. I would like to thank Dr. Reza Ghaffarian for his encouragement and support. This work is supported by NEPP to assess the reliability of the package.

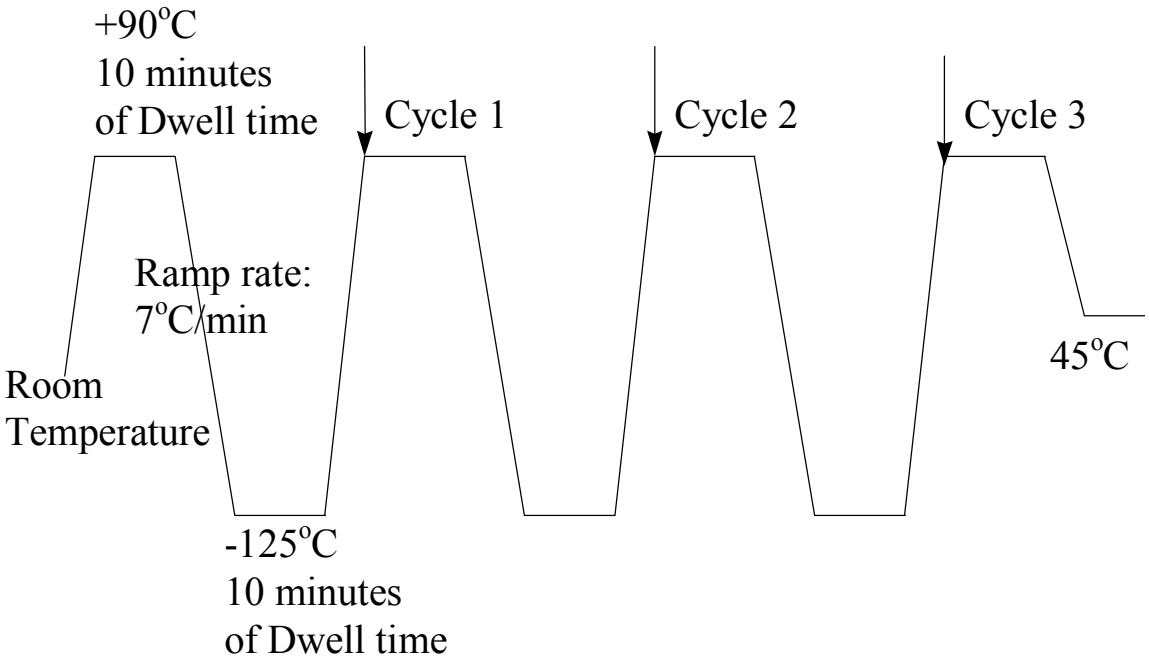


Figure 1. Thermal cycle profile employed for thermal cycling.

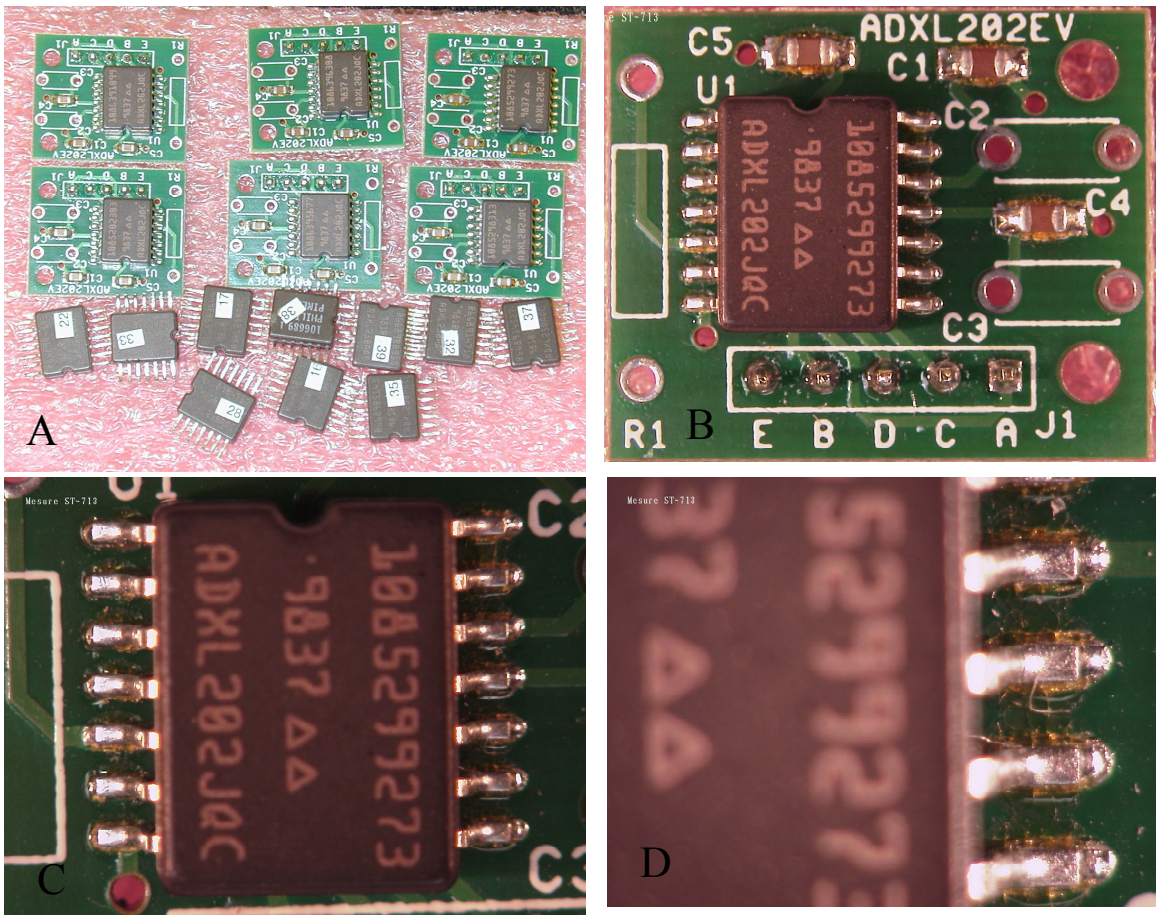


Figure 2. Optical photographs of the some of the test vehicles with ADXL 202 and ADXL250 accelerometers.

S/N	Vout X	Vout Y	Self-Test X	Self-Test Y	Sen X	Sen Y	Supply I
16	2.4325v	2.5039v	342.1mV	336.6mV	36.7mV	38.4mV	2.98 mA
17	2.4122v	2.4495v	324.2mV	324.5mV	35.7mV	34.6mV	2.84 mA
22	2.5170v	2.4679v	356.1mV	355.4mV	35.3mV	33.9mV	2.71 mA
28	2.4881v	2.5561v	344.6mV	363.8mV	36.2mV	34.9mV	2.78 mA
32	2.3449v	2.5037v	324.6mV	332.5mV	39.2mV	36.2mV	2.62 mA
33	2.4357v	2.4402v	335.1mV	331.5mV	37.3mV	36.5mV	2.78 mA
35	2.3583v	2.4319v	337.0mV	316.4mV	36.7mV	38.6mV	2.89 mA
37	2.4006v	2.4318v	338.6mV	338.5mV	38.8mV	37.2mV	2.85 mA
38	380mV	-536mV					.13 mA
39	2.4096v	2.3962v	332.2mV	329.7mV	35.9mV	34.1mV	2.80 mA

Table 1. ADXL 250 Analog Devices Dual Axis Accelerometer electrical characteristics after 27 extreme temperature thermal cycling (-120 ^{o}C to 90 ^{o}C).

S/N	Sensitivity X	Y	Iq	Rin	Output change	Zero G bias level output bias voltage X	Y
16	37.9mV	37.9mV	2.88 mA	53 K	0.340V	2.4558V	2.5064V
17	37.4 mV	35.0 mV	2.81 mA	54K	0.324V	2.4173V	2.4516V
22	36.2 mV	34.0 mV	2.71 mA	55K	0.358V	2.5351V	2.4849V
28	37.5 mV	35.3 mV	2.78 mA	55K	0.345V	2.4985V	2.5462V
32	39.0 mV	36.2 mV	2.61 mA	56K	0.325V	2.3664V	2.5047V
33	37.0 mV	35.8 mV	2.78 mA	55K	0.335V	2.4419V	2.4397V
35	37.3 mV	39.0 mV	2.89 mA	53K	0.337V	2.3719V	2.4350V
37	39.6 mV	37.0 mV	2.85 mA	53K	0.338V	2.4212V	2.4446V
39	37.2 mV	34.4 mV	2.80 mA	54K	0.335V	2.4126V	2.4084V

Table 2. ADXL 250 Analog Devices Dual Axis Accelerometer electrical characteristics after 61 extreme temperature thermal cycling (-120 ^{o}C to 90 ^{o}C).

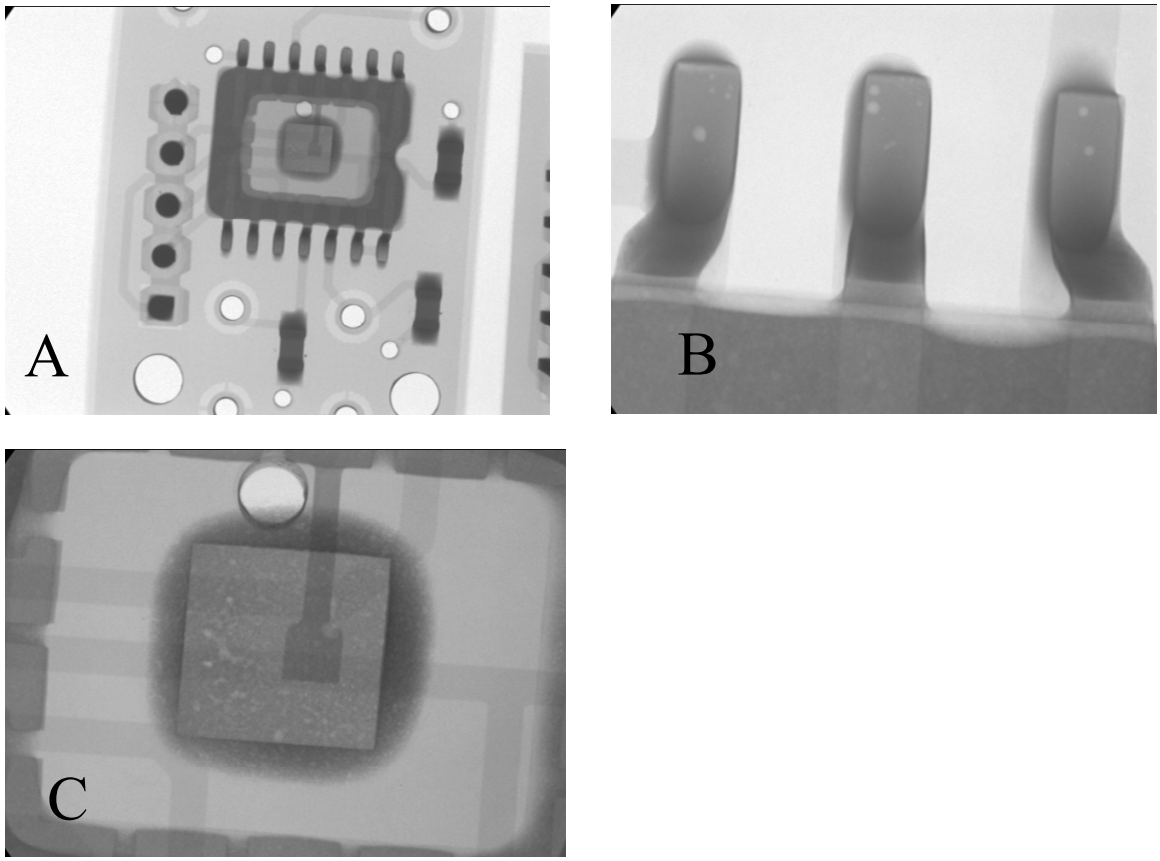


Figure 3. Typical X-ray images of the sensors shown in Figure 2B.

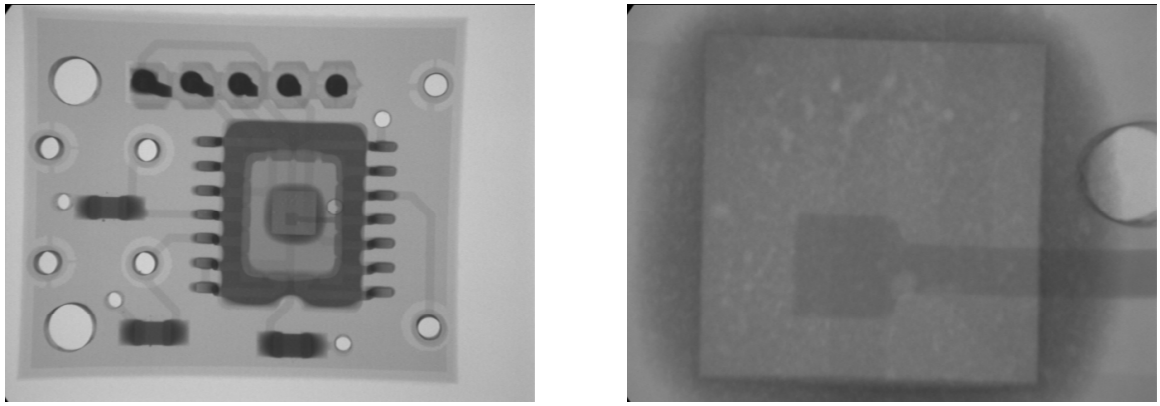
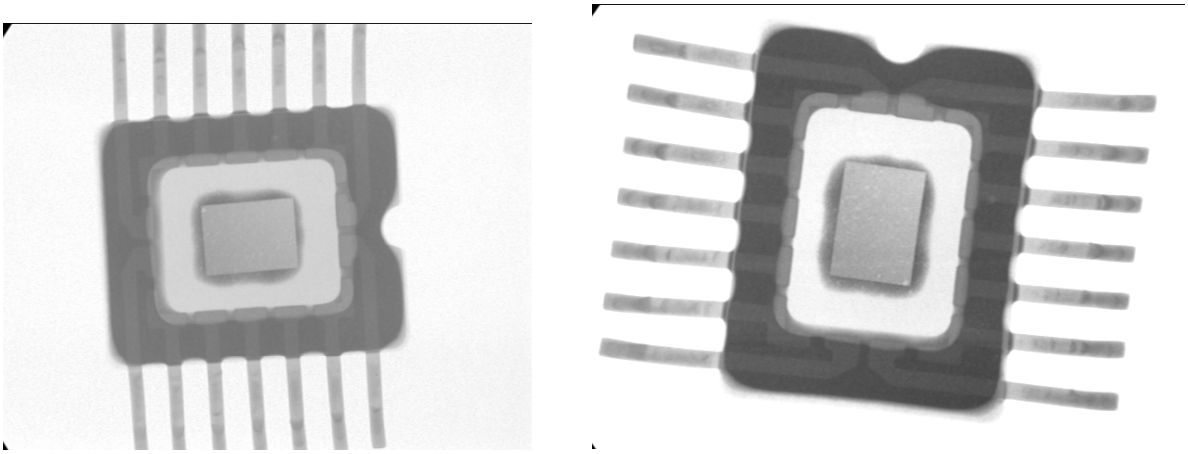


Figure 4. X-ray images of the sensors shown in Figure 2B after 23 extreme thermal cycles.



A B

Figure 5. X-ray image of the ADXL250 accelerometer A (before) and B (after) 61 extreme temperature thermal cycles.

Assessment of Advanced Flip-Chip Electronics Package Test Assemblies Under Extreme Temperatures

Rajeshuni Ramesham, NASA JPL/California Institute of Technology
Rajeshuni.Ramesham@jpl.nasa.gov, 818.354.7190

Abstract

FB250 and FB500 flip-chip boards have been assembled and subjected to extreme temperature thermal cycling in order to evaluate the robustness of this advanced packaging technology. The temperature range covers military specifications and the extreme Martian environment at various ramp rates. Resistance of the daisy chained flip chips has been monitored as a function of thermal cycling. Preliminary electrical resistance measurements have been reported; electrical tests to date have not shown significant change in resistance as a function of thermal cycling. However, the greater the number of thermal cycles, the more noticeable the change in the resistance of the daisy chained flip chips. No catastrophic failures were observed, even after 481 extreme temperature thermal cycles per electrical measurements. However, process qualification is required to optimize the flip-chip assembly.

Flip-Chip Test Boards

With an increasing number of I/Os on integrated circuits and accompanying requirements for high performance, flip-chip type components have become a compelling technology. NASA will be one of their primary users, especially in the context of wide extreme temperature ranges. We have the ability to test boards for die specifications, bump pitches, and bump counts; both components and test boards are daisy chained for continuity. Figure 1 shows the optical photographs of the FB250 and FB500 test boards: High temperature FR4 (T_g = 176 ^oC) 0.031" thickness, copper conductor, Taiyo PSR-400 solder mask, FB250 board (10: 250 x 250 mil^2 sites, pitch 18 mil, minimum line 6 mil, and maximum space 12 mil), and FB500 board (10: 500 x 500 mil^2 sites, pitch 18 mil, minimum line 6 mil, and maximum space 12 mil).

Temperature Profile

Figure 2 shows the temperature profile employed to perform the extreme temperature thermal cycling of the FB250 and FB500 flip-chip test boards.

1. Baseline: at room temperature, 25 ^oC.
2. TC1 cover tow ranges:
    a. 281 cycles in a temperature range of (X) -120 ^oC to +115 ^oC; Y: ramp rate of 5 ^oC/minute.
    b. 200 cycles in a temperature range of (X) -120 ^oC to +85 ^oC; Y: ramp rate of 5 ^oC/minute.
3. TC2 cover tow ranges: 200 cycles in a temperature range of (X) -55 ^oC to +100 ^oC; Y: ramp rate of 5 ^oC/minute (mil spec).
4. TC1 cover tow ranges: 100 cycles in a temperature range of (X) -120 ^oC to +85 ^oC; Y: ramp rate of 40 ^oC/minute.

Electrical Tests

The resistance of the daisy chained FB250 and FB500 test boards (Figure 1) was measured as a function of thermal cycling performed in the various temperature ranges described above. Figures 3 and 4 show the experimental test data after thermal cycling. Detailed experimental data will be presented in the future.

X-ray Imaging and Surface Acoustic Microscopy

This work will be performed shortly to identify failures in the flip-chip interconnects as a function of thermal cycling in an extreme temperature range. Electrical tests show that there is not significant change in resistance as a function of thermal cycling.

FB500

Bare chip inspection: The X-ray image of one chip is shown in Figure 5. Two opposite corners, depicted at the same magnification, show non-uniform solder bumping.

Solder wetting after reflow: Kester 6502 tacky flux with a shim of 35μm thickness was used for this build. The X-ray image of a solder joint after reflow is shown in Figure 6; this figure represents two opposite corners at the same magnification, showing different wetting results. The cross-section images of the two adjacent edges corresponding to Figure 6(b) are shown in Figure 7.

Underfill: Parameters for the underfill process are shown in Table 1. The CSAM images were obtained after underfill cure. One out of 40 chips was found with voids, which is shown in Figure 8. The middle line pattern with one-third of the edge length was used for dispensing. The void occurred close to the opposite edge.

FB250

Solder wetting after reflow: Kester 6502 tacky flux with a shim of 35μm thickness was used for this build. The X-ray image of a solder joint after reflow is shown in Figure 9. The shape of the solder joint indicates good wetting.

Underfill: Parameters for the underfill process are shown in Table 2. The CSAM images were obtained after underfill cure. Four out of 70 chips were found with voids, which are shown in Figure 10. The middle line pattern with one-third of the edge length was used for dispensing. The void occurred close to the opposite edge.

Conclusions

Advanced packaging technology, such as flip-chip test boards (FB250 and 500), has been subjected to extreme temperature ranges that cover military specifications and the extreme Martian environment at various ramp rates. The greater the number of thermal cycles, the more

noticeable the change in resistance of the daisy chained flip chips. No catastrophic failures were observed, even after 481 extreme temperature thermal cycles per electrical measurements. Process qualification is required to optimize the flip-chip assembly, which is clear from the X-ray and CSAM studies. X-ray and CSAM studies have not been made as of yet after thermal cycling and will be done shortly. After extensive testing for future space applications in the extreme temperature environments, it may be determined that the flip-chip advanced test assembly is a robust technology.

Acknowledgements

This work has been supported by NEPP to assess the reliability of advanced interconnect and packaging technologies under extreme cold temperatures. I would like to thank Dr. Reza Ghaffarian for his encouragement and support.

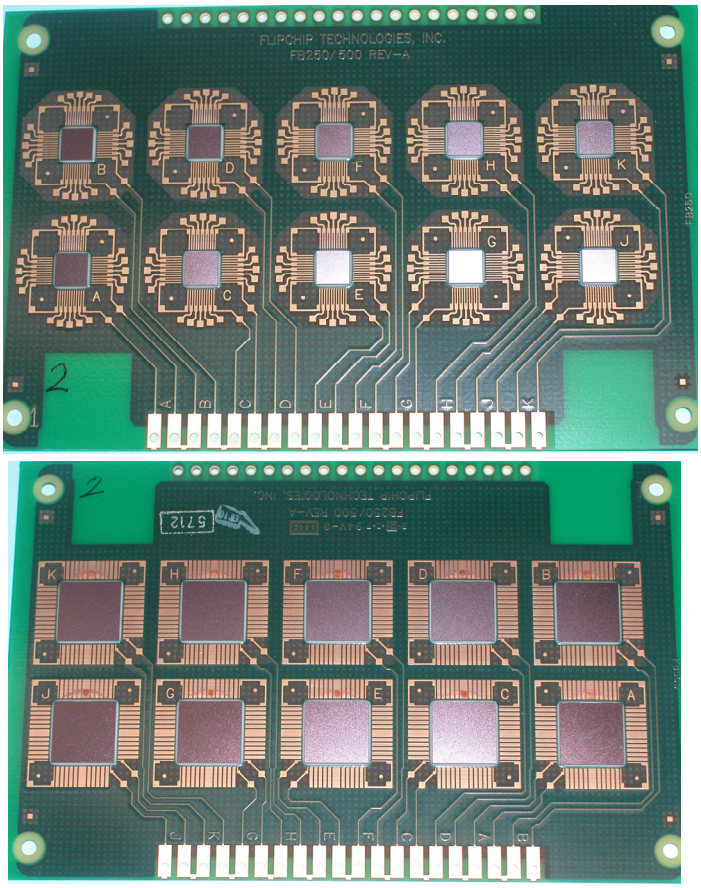


Figure 1. Optical photographs of the flip-chip test boards of FB250 and FB500.

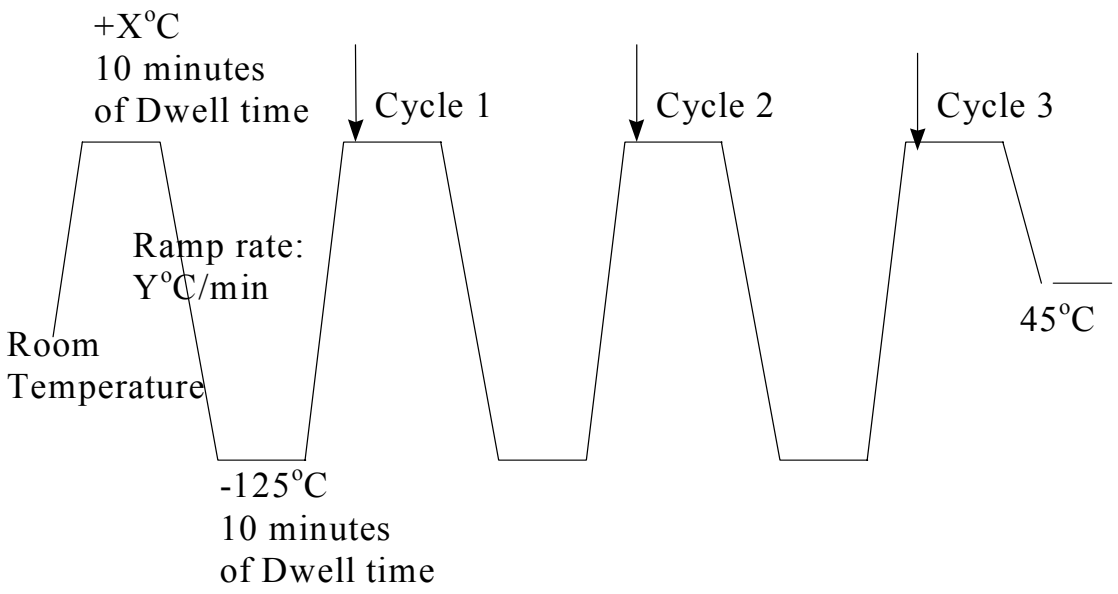


Figure 2. Thermal cycle test profile employed for various temperature ranges of thermal cycling.

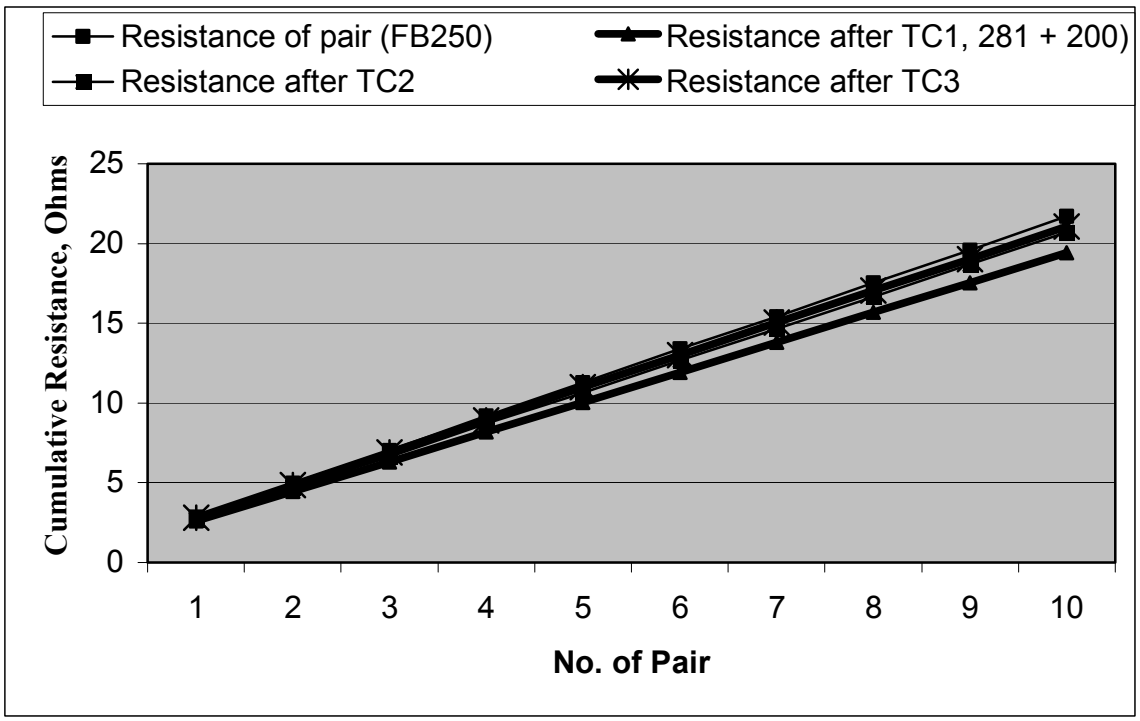


Figure 3. Resistance of the daisy chained flip-chip FB250 test board: a. Resistance of the pairs at room temperature, b. resistance of the pairs measured after 481 thermal cycles -120 °C to 115 °C and -120 °C to 85 °C (TC1), c. resistance of the pairs measured after 200 thermal cycles -55 °C to 100 °C (TC2), and d. resistance of the pairs measured after 100 thermal cycles -125 °C to 85 °C (TC3).

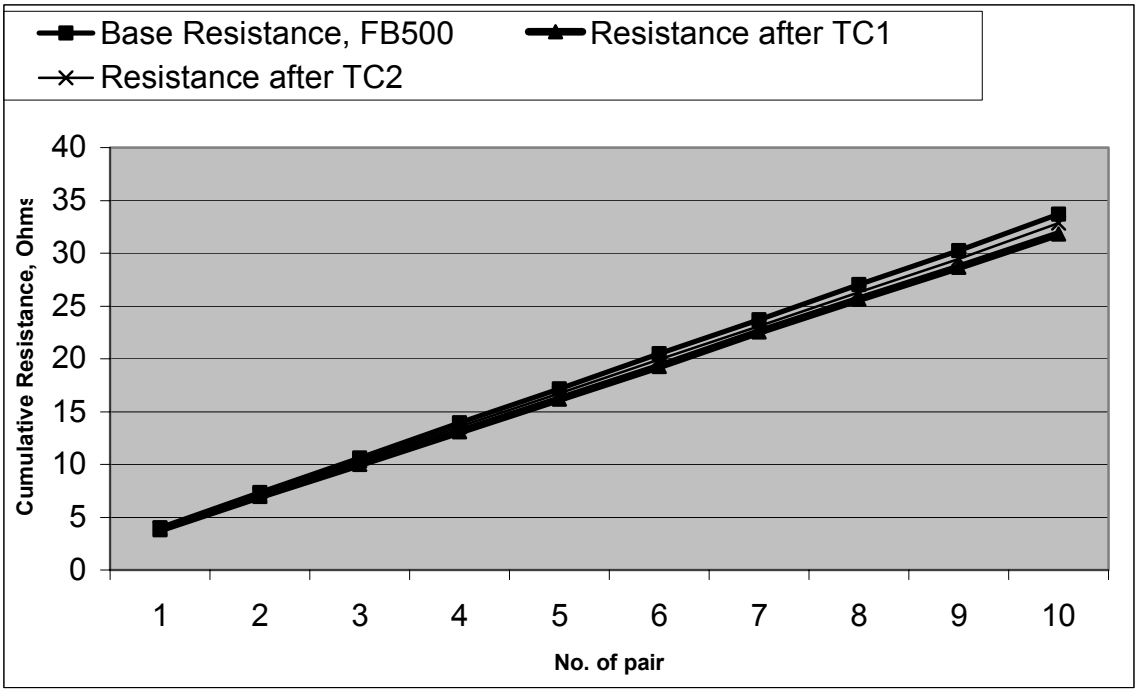


Figure 4. Resistance of the daisy chained flip-chip FB500 test board: a. Resistance of the pairs at room temperature, b. resistance of the pairs measured after 481 thermal cycles -120 ^{o}C to 115 ^{o}C and -120 ^{o}C to 85 ^{o}C (TC1), and c. resistance of the pairs measured after 200 thermal cycles -55 ^{o}C to 100 ^{o}C (TC2).

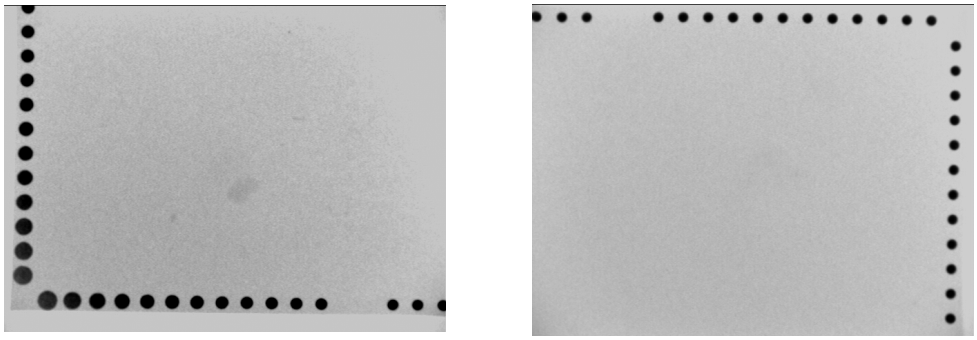
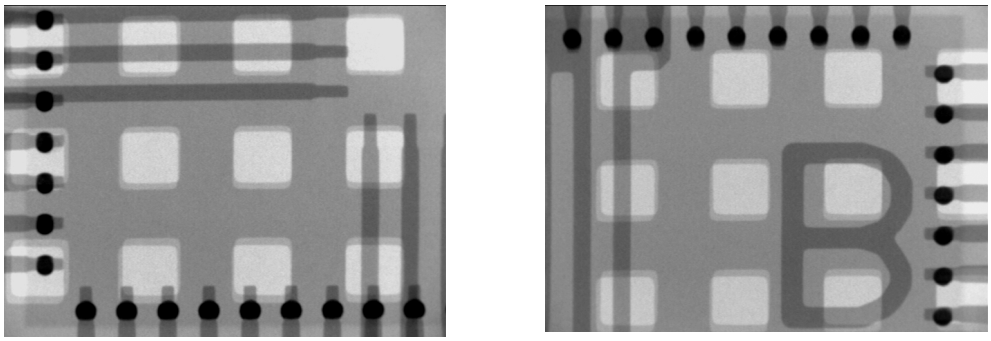
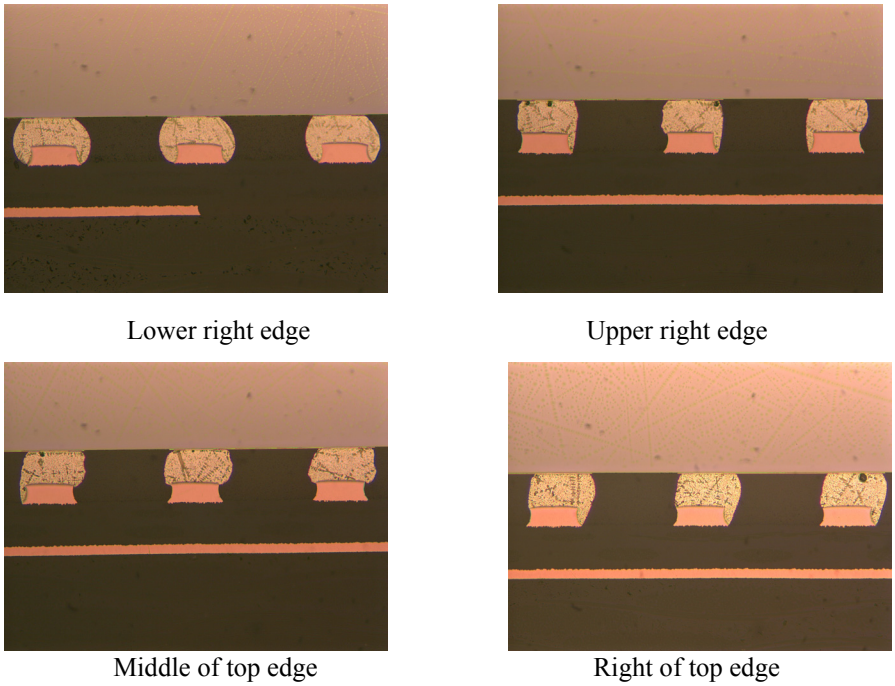


Figure 5. X-ray image of a bare chip at two opposite corners.



(a) (b)

Figure 6. X-ray image of solder wetting after reflow.



Lower right edge Upper right edge

Middle of top edge Right of top edge

Figure 7. Cross section of top right corner, viewed from chip side.

Underfill	Stage temp. (°C)	Air pressure (psi)	Needle gauge	RPM	Line speed (in/sec)
RDP-960	80	6	#23	250	0.08

Table 1. Parameters for underfill component FB500.

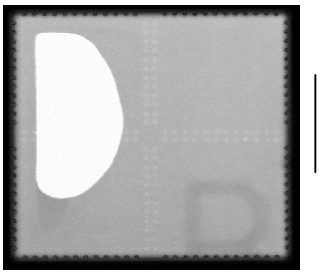


Figure 8. CSAM image of underfill with void (board 3, die C).

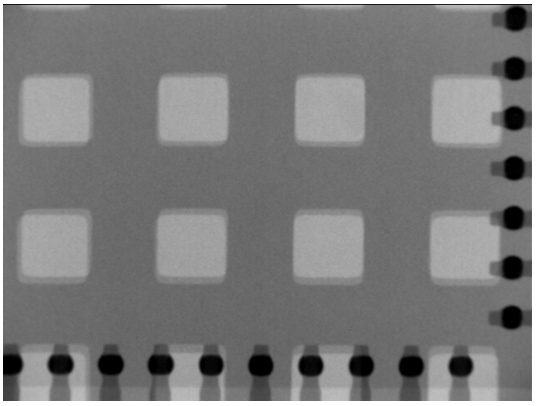
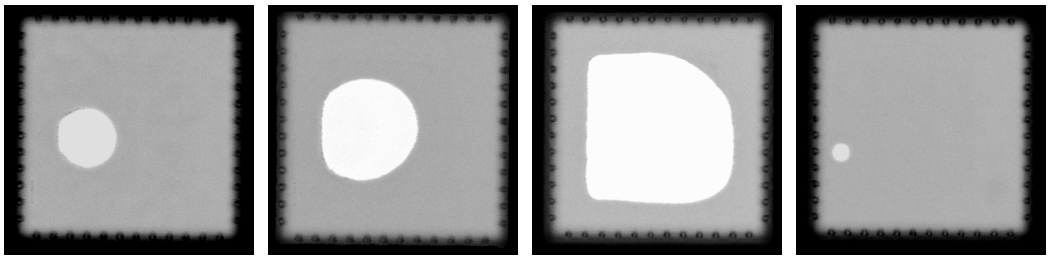


Figure 9. X-ray image of solder wetting after reflow.

Underfill	Stage temp. (°C)	Air pressure (psi)	Needle gauge	RPM	Line speed (in/sec)
RDP-960	100	6	#23	250	0.08

Table 2. Parameters for underfill component FB250.



Board1_D Board5_E Board7_D Board7_F

Figure 10. CSAM images of underfill with voids.

High Temperature Electronics: A Role for Wide Bandgap Semiconductors?

Philip G. Neudeck, NASA GRC, neudeck@grc.nasa.gov
Robert S. Okojie, NASA GRC, Cleveland, Ohio 44135
Liang-Yu Chen, NASA GRC, Liangyu.Chen@grc.nasa.gov

Abstract

It is recognized increasingly that semiconductor based electronics that can function at ambient temperatures higher than 150 °C without external cooling could greatly benefit a variety of important applications, especially in the automotive, aerospace, and energy production industries. The fact that wide bandgap semiconductors are capable of electronic functionality at much higher temperatures than silicon has partially fueled their development, particularly in the case of SiC. It appears unlikely that wide bandgap semiconductor devices will find much use in low-power transistor applications until the ambient temperature exceeds approximately 300 °C, as commercially available silicon and silicon-on-insulator (SOI) technologies are already satisfying requirements for digital and analog VLSI circuits in this temperature range. However, practical operation of silicon power devices at ambient temperatures above 200 °C appears problematic, as self-heating at higher power levels results in high internal junction temperatures and leakages. Thus, most electronic subsystems that simultaneously require high temperature and high power operation will be realized necessarily using wide bandgap devices, once the technology for realizing these devices becomes developed sufficiently for wide availability. Technological challenges impeding the realization of beneficial wide bandgap high ambient temperature electronics, including material growth, contacts, and packaging, are briefly discussed.

To view the full-length article, see the June 2002 issue of Proceedings of the IEEE.

Microsystem Packaging for High Temperature Environments

Liang-Yu Chen, OAI/NASA GRC, Liangyu.Chen@grc.nasa.gov

Patrick McCluskey, Department of Mechanical Engineering, University of Maryland, College Park

Abstract

Microsystems composed of microelectronics and micro-electro-mechanical systems (MEMS) are being considered increasingly for high temperature applications, such as aerospace engine monitoring and space exploration. While electronic and MEMS devices exist to perform the needed functions, little attention has been paid to the packaging technology for high temperature environment operation. This paper discusses the issues involved in high temperature packaging of microsystems, and describes a ceramic chip level package developed and evaluated by NASA Glenn Research Center.

Introduction

Cost, size, weight, and performance advantages have driven the incorporation of distributed control systems in aircraft and automobiles in the past few years. Such systems require microelectronics that can operate at temperatures well above the traditional maximum allowable operating temperatures of 70 °C for commercial electronics and 125 °C for military electronics [1]. Interest is now growing in utilizing microsystems composed of electronics and MEMS sensors/actuators in these high temperature applications, where these microsystems may, in fact, see temperatures significantly higher than the upper limits for conventional electronics.

NASA is especially interested in using high temperature microsystems. Here the desire is to perform in situ characterization of the combustion processes of aerospace engines and of the atmosphere of inner solar planets such as Venus. In aeronautic engine applications, the microsystems must operate at temperatures up to 500 °C and under pressures up to 20 MPa in a gas ambient composed of chemically reactive species such as oxygen (in air) and hydrocarbon/hydrogen (in fuel), along with catalytically poisoning species such as NOx and SOx from combustion products. The microsystems needed to characterize the atmosphere of Venus must operate in acid gas at 500 °C under 9 MPa. For a landing space probe, the microsystems must also withstand high (de)acceleration.

These are indeed high temperature environments compared to the standard operating conditions for most commercial sensors/electronics. In addition to the basic electronics for signal conditioning and intelligent control, these applications require pressure sensors, gas flow sensors, gas chemical sensors, and accelerometers. In recent years, silicon carbide (SiC) high temperature electronic and MEMS devices that can perform these functions have been demonstrated; however, most of these devices were demonstrated in laboratory conditions because packaging technology was not available. High temperature packaging technology is thus a key element of in situ testing and commercialization of high temperature operable microsystems.

When addressing packaging for high temperature environments, the design elements and materials used must be selected for their ability to perform their intended function over time in the high temperature environment. For example, in NASA's high temperature applications, the

substrate, metallization material(s), electrical interconnections, and die-attach must in each case be able to withstand 500 °C temperature, chemically corrosive gases, high dynamic pressure, and high acceleration. Much of the work that has gone into developing packaging for high temperature electronic control systems can be utilized to develop microsystem packages. Each of these elements is described in further detail below.

Die Attach

Microsystems are, at least partially, mechanical devices, and as such are sensitive to external mechanical forces. A major external force that can act on a microsystem is the thermo-mechanical stress arising from thermal expansion mismatches between the die, die attaching (bonding) layer, and the substrate. This thermally induced stress can generate unwanted device response to temperature changes, and, in the extreme case, permanent mechanical damage to the die attach. This stress must be minimized, through careful selection of the die attach, to achieve precise and reliable device operation.

Commercial plastic encapsulated microelectronics use silver-filled epoxies to attach the die to the substrate. Epoxies minimize the stress on the die, but degrade at temperatures before reaching 200 °C, thereby eliminating them as candidates for use in high temperature microsystems. The alternatives are silver-filled glasses and solders. Silver-filled glasses are quite stiff, often placing considerable thermomechanical stress on the chip. Therefore, for 200 °C applications, the best alternatives appear to be solders. There are several high temperature solders that have been used successfully as die attaches, including Pb95Sn05, Pb90Sn10, 95Sn5Sb, and Sn65Ag25Sb10. Gold-based eutectic alloys are another option for high temperature die attach. These alloys have excellent creep and corrosion resistance together with high strength; however, their stiffness causes them to transmit most of the thermo-mechanical stress to the die, as with silver-filled glasses [2], and they are soft at temperatures above 400 °C. Gold (Au) thick-film material has been tested as die attaching material for 500 °C applications.

Substrates and Metallization

Ceramic substrates and precious metal thick-film metallization have been proposed for chip level packaging of high temperature and other harsh environment devices based on their excellent stabilities at high temperatures and in chemically reactive environments [3, 4]. Three ceramic materials are typically used as substrates for high temperature microsystems: aluminum oxide, beryllium oxide, and aluminum nitride. Aluminum oxide (Al_2O_3) is the cheapest and has a reasonable thermal expansion match to SiC and silicon (Si), but it has poor thermal conductivity. Beryllium oxide (BeO) has a significantly higher thermal conductivity, but its thermal coefficient of thermal expansion (7.2) provides a poorer match to silicon, increasing the thermomechanical stresses induced during power or thermal cycling. Other drawbacks include its high cost and potential toxicity. The third alternative, alumimum nitride (AlN), combines the best expansion match to SiC and Si with the thermal conductivity of BeO [5]. In recent years, its cost has declined and issues related to its metallization have been solved, thus rendering it the substrate of choice for high temperature microsystems [4].

Wirebonds and Flip Chip Attachment

High temperature applications can weaken both the wire and the wirebond by annealing the wire and causing intermetallic reactions at the bond site, respectively. Annealing increases the grain size in the wire, reducing the wire's strength and fatigue resistance. Intermetallic reaction can lead to the formation of voids and brittle compounds that cause fatigue fracture at the bond interface. Intermetallic formation is most often seen at temperatures exceeding 125 °C in Au wire/aluminum (Al) bond pad, interconnects [2]. Other wirebond systems, such as Al wire/nickel (Ni) bond pad, have a slower rate of intermetallic formation, and thus a higher allowable use temperature [6]. Temperatures in excess of 300 °C require monometallic wirebond systems such as Al wire/Al bond pad or Au wire/Au bond pad.

In order to achieve higher packaging density, in many cases, microsystem electronics are directly joined to the substrate by flip chip solder joints instead of wirebonds. The high lead solders used in flip chip joints will not degrade at temperatures up to 250 °C. Nevertheless, the CTE mismatch between the microsystem (chip), die-attaching material, and the substrate must be kept low, as the underfills typically used to lower thermomechanical stress in commercial ICs are not stable above 150 °C [7].

Issues Unique to High Temperature Microsystems

There are also a host of packaging issues that are unique to microsystems. Thermal expansion can narrow or widen tolerance gaps, leading to interferences or loose joints, respectively. For example, thermal expansion can cause jamming of the mechanical feed-through for an actuator, or conversely cause an opening in the gasket of the feed-through so that it no longer provides a seal to protect the electronics inside the package. Another possible effect of temperature is to change the internal diameter of microfluidic tubes thereby affecting the flow rate and the measurement of fluid flow. Such effects would need to be considered in design and calibration.

Elevated temperatures also accelerate chemical reactions. This can affect sensor chips not only by increasing the rate of environmentally-induced sensor degradation, but also by increasing the sensing reaction rate in a manner similar to having a higher level of the sensed chemical, thereby requiring re-calibration. In the limit, it is possible that elevated temperatures might change the nature of the chemical reaction that is used by the sensor, rendering it inoperable.

NASA Ceramic Packages

Researchers at NASA Glenn Research Center have developed chip level prototype electronic packages for high temperature and other harsh environment microsystems using AlN and Al2O3 ceramic substrates and gold (Au) thick-film metallization (see Figure 1). The electrical interconnection system of this advanced packaging system, including the thick-film metallization and wirebonds, has been successfully tested in a 500 °C oxidizing environment for over 5,000 hours. A compatible low resistance die-attach scheme using Au thick-film material as a conductive bonding material was also developed that is compatible with SiC devices [8]. This complete electrical interconnection system was tested with an in-house-fabricated SiC Schottky diode test chip in an oxidizing environment in a temperature range from room temperature to 500 °C for more than 1,000 hrs. These test results set lifetime records for both high temperature electronic packaging and high temperature electronic device testing. As required, the thick-film-based interconnection system demonstrated electrical resistance characteristics that were both

low (2.5 times the 25 °C resistance of the Au conductor) and stable (decreased 3% in the first 1,500 hrs. of continuous testing) at 500 °C in an oxidizing environment. Also as required, the electrical isolation impedance between printed conductors/wires of the prototype packages (shown in Figure 1) remained high (>0.4 GW) at 500 °C in air. The attached SiC diode demonstrated low (< 3.8 W- mm2) and relatively consistent forward dynamic resistance from room temperature to 500 °C as indicated by Figure 2. These results indicate that this prototype package meets the design requirements for low power, long term operation in high temperature, chemically corrosive environments. This technology will be further developed and evaluated for packaging various SiC high temperature microsystems.

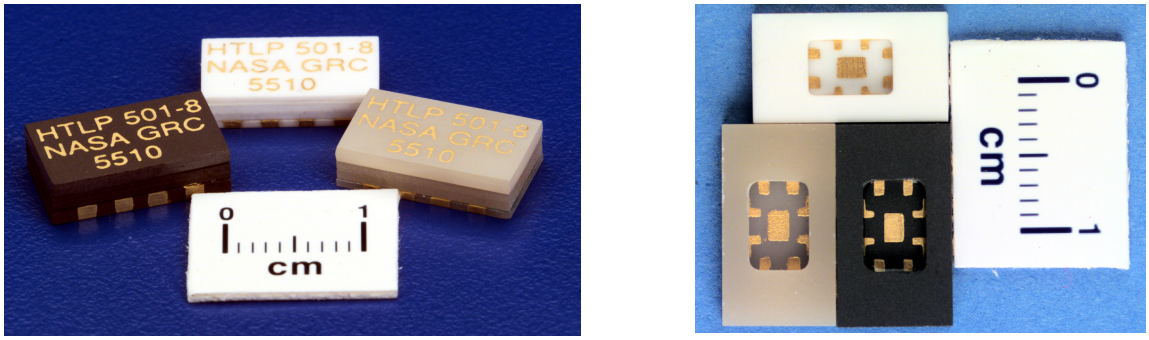


Figure 1. Prototype high temperature SiC microsystem electronic package.

Conclusion

In conclusion, packaging of microsystems for temperatures as high as 500 °C has been demonstrated. However, it requires very careful attention to material compatibility issues and design tolerances. Furthermore, package design can vary from the simple to the complex based on the amount of interaction between the microsystem and the environment. As a result, further research is needed to lower the cost, improve the reliability, and increase the flexibility of microsystem packaging for high temperature applications.

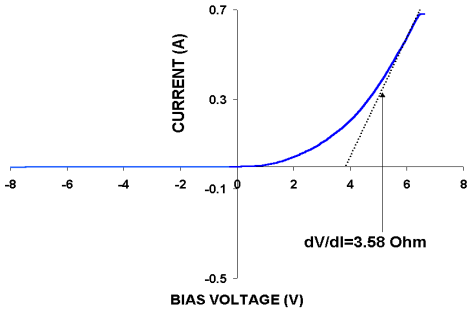


Figure 2. I-V curve of a packaged SiC diode, using Au thick-film material as die-attach layer, characterized at 500 °C after 1,000 hrs. test at 500 °C [4].

Acknowledgments

The authors would like to acknowledge the more than 50 members of the CALCE Electronic Products and Systems Center for their support of this research. They would also like to thank the NASA Electronic Parts and Packaging (NEPP) Program, the Glennan Microsystems Initiative (GMI), the DARPA High Temperature Distributed Control Systems TRP, and the ONR PEBB Program for their support. For more information on high temperature MEMS research at NASA Glenn, please contact Dr. Lawrence G. Matus at NASA Glenn Research Center, Cleveland, OH 44135. For more information on high temperature microsystems research at CALCE, please contact Dr. Patrick McCluskey.

References

[1] C. M. Carlin and J. K. Ray, "The Requirements for High Temperature Electronics in a Future High Speed Civil Transport," Proceedings of the 2nd International High Temperature Electronics Conference, held in Charlotte, NC, June 1994, p. I-9.

[2] F. P. McCluskey, D. Das, J. Jordan, L. Condra, T. Torri, J. Fink, and R. Grzybowski, "Packaging of Electronics for High Temperature Environments," International Journal of Microcircuits and Electronic Packaging, Vol. 20, No. 3, p. 409, Third Quarter 1998.

[3] J. S. Salmon, R. W. Johnson, and M. Palmer, "Thick Film Hybrid Packaging Techniques for 500oC Operation," Proceedings of 4th International High Temperature Electronics Conference, held in Albuquerque, NM, June 1998.

[4] L.-Y. Chen, R. S. Okojie, P. G. Neudeck, G. W. Hunter, and S.-T. Lin, "Material System for Packaging 500oC MicroSystem," MRS 2001 Spring Meeting Proceedings- Microelectronic, Optoelectronic, and MEMS Packaging (Symposium N), held in San Francisco, CA, April 2001.

[5] H. K. Charles, Jr., and G. V. Clatterbaugh, "Packaging Considerations for High Temperature Operation," Proceedings of the 2nd International High Temperature Electronics Conference, held in Charlotte, NC, June 1994, p. IX-3.

[6] J. Benoit, S. Chin, R. Grzybowski, S. Lin, R. Jain, and P. McCluskey, "Wire Bond Metallurgy for High Temperature Electronics," Proceedings of the 4th International High Temperature Electronics Conference, held in Albuquerque, NM, June 1998, p. 109.

[7] R. W. Johnson, Tutorial Session, 5th International High Temperature Electronics Conference, held in Albuquerque, NM, June 2000.

[8] L.-Y. Chen, G. W. Hunter, and P.G. Neudeck, "Silicon Carbide Die Attach Scheme for 500oC Operation," MRS 2000 Spring Meeting Proceedings-Wide-Bandgap Electronic Devices (Symposium T), held in San Francisco, CA, April 2000.

Characterizing Space Flight Inductors and Transformer Failures

Ben Oni, Ph.D., NASA MSFC/Tuskegee University
Trent Griffin, Karen Cunningham, Bob Kapustka, and Steve Luna, NASA MSFC, Huntsville, Alabama 35812

Abstract

Various design and manufacturing standards are generally imposed on space flight hardware development processes with the objective to reduce failure risks. In spite of these standards, some chip scale package (CSP) assemblies and discrete components used in power electronics hardware developments still fail in use and require understanding of the failure mechanisms to establish improved confidence in reliability. Failures of space flight inductors and transformers, developed to MIL-STD 981, were studied. The paper characterized the failures in terms of type, cause, method of detection, and frequency of occurrences.

The principal objective for the characterization was to see if there are correlations between the type of failures and the testing and/or analysis that is or is not performed. If it could be determined that the performance of certain tests and/or analyses on power electronics hardware greatly enhance mission success and that the performance of other tests and/or analyses do not, then one would be able to better advise the customer on which test and/or analysis options would give the best value.

Available records, over the last 32 years, of failure data on space flight inductors and transformers were sought from several sources and analyzed. The sources included the Government Industry Data Exchange Program (GIDEP), NASA Reliability Preferred Practices for Design and Test regarding Lessons Learned Information, Magnetics Manufacturers, and Electronic Screening Houses.

The paper also presents the relative importance of the various MIL-STD 981 tests, as perceived by manufacturers of inductors and transformers.

Conclusions

Based on the available GIDEP data used in this analysis, the following conclusions were made:

1. Magnetic components fail more in the open circuit mode than in the short circuit mode.
2. More failures result from manufacturing errors than from design or installation errors.
3. Advances in manufacturing technology do not show decline in manufacturing related failures with years.
4. More components fail the thermal cycle test than other tests.
5. About 20% of failures occur in use.
6. Failure occurring in use is caused by a number of reasons; however, insulation breakdown and improper solder joints are more prevalent causes.

On the relative importance of MIL-STD 981 tests as perceived by manufacturers of inductors and transformers, the following conclusions were made:

7. Tests performed depend on customer applications.
8. Irrespective of application, the majority of magnetics manufacturers consider dielectric and electrical tests as highest priority.
9. Seal and radiographic tests were generally considered least critical. It is noted, however, that in some applications, these tests may be absolutely necessary.

The full-length paper is posted on the NEPP Web site at http://nepp.nasa.gov/index_nasa.cfm/619/410ED5D3-29D9-4B45-B4842D442EF27444/.